LANSDALE Semiconductor, Inc.

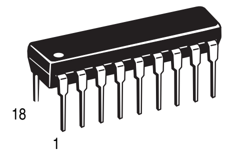
ML145145
4–Bit Data Bus Input PLL Frequency Synthesizer

INTERFACES WITH SINGLE–MODULUS PRESCALERS

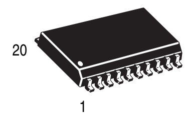
Legacy Device: *Motorola MC145145-2*

The ML145145 is programmed by a 4–bit input, with strobe and address lines. The device features consist of a reference oscillator, 12–bit programmable reference divider, digital phase detector, 14–bit programmable divide–by–N counter, and the necessary latch circuitry for accepting the 4–bit input data.

- Operating Temperature Range: T_A – 40 to 85°C
- Low Power Consumption Through the Use of CMOS Technology
- 3.0 to 9.0 V Supply Range
- Single Modulus 4–Bit Data Bus Programming
- ÷N Range = 3 to 16,383, ÷R Range = 3 to 4,095
- “Linearized” Digital Phase Detector Enhances Transfer Function Linearity
- Two Error Signal Options:
  - Single–Ended (Three–State)
  - Double–Ended



P DIP 18 = VP
PLASTIC DIP
CASE 707



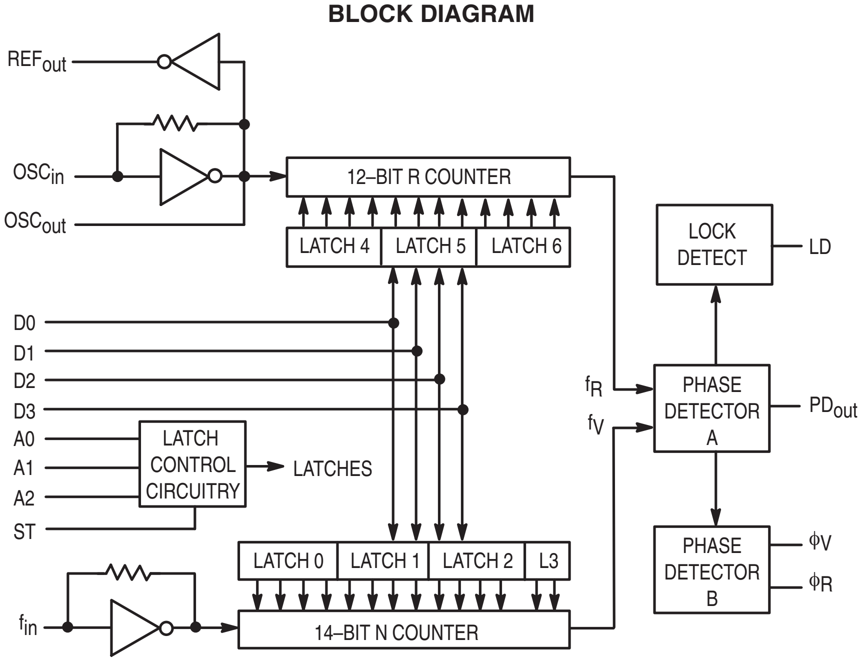
SOG 20 = -6P
SOG PACKAGE
CASE 751D

CROSS REFERENCE/ORDERING INFORMATION

PACKAGE	MOTOROLA	LANSDALE
P DIP 18	MC145145P1	ML145145VP
SOG 20	MC145145DW2	ML145145-6P

Note: Lansdale lead free (**Pb**) product, as it becomes available, will be identified by a part number prefix change from **ML** to **MLE**.

BLOCK DIAGRAM



PIN ASSIGNMENTS

PLASTIC DIP

1	D1	18	D2
2	D0	17	D3
3	f_{in}	16	REF_{out}
4	V_{SS}	15	ϕR
5	V_{DD}	14	ϕV
6	OSC_{in}	13	LD
7	OSC_{out}	12	PD_{out}
8	A0	11	ST
9	A1	10	A2

SOG PACKAGE

1	D1	20	D2
2	D0	19	D3
3	NC	18	REF_{out}
4	f_{in}	17	ϕR
5	V_{SS}	16	ϕV
6	V_{DD}	15	LD
7	OSC_{in}	14	PD_{out}
8	OSC_{out}	13	ST
9	A0	12	A2
10	A1	11	NC

NC = NO CONNECTION

MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	−0.5 to +10	V
V_{in}, V_{out}	Input or Output Voltage (DC or Transient)	−0.5 to V_{DD}+0.5	V
I_{in}, I_{out}	Input or Output Current (DC or Transient), per Pin	±10	mA
I_{DD}, I_{SS}	Supply Current, V_{DD} or V_{SS} Pins	±30	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	−65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds	260	°C

* Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics tables or Pin Descriptions section.

†Power Dissipation Temperature Derating:
Plastic DIP: −12 mW/°C from 65 to 85°C
SOG Package: −7.0 mW/°C from 65 to 85°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to these high–impedance circuits. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}), except for inputs with pull–up devices. Unused outputs must be left open.

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Symbol	Parameter	Test Conditions	V_{DD} V	−40°C		25°C		85°C		Unit
				Min	Max	Min	Max	Min	Max	
V_{DD}	Power Supply Voltage Range		—	3.0	9.0	3.0	9.0	3.0	9.0	V
I_{ss}	Dynamic Supply Current	f_{in} = OSC_{in} = 10 MHz, 1 V p–p ac coupled sine wave R = 128, A = 32, N = 128	3.0 5.0 9.0	— — —	3.5 10 30	— — —	3.0 7.5 24	— — —	3.0 7.5 24	mA
I_{SS}	Quiescent Supply Current	V_{in} = V_{DD} or V_{SS} I_{out} = 0 µA	3.0 5.0 9.0	— — —	800 1200 1600	— — —	800 1200 1600	— — —	1600 2400 3200	µA
V_{in}	Input Voltage — f_{in}, OSC_{in}	Input ac coupled sine wave	—	500	—	500	—	500	—	mV p–p
V_{IL}	Low–Level Input Voltage — f_{in}, OSC_{in}	V_{out} ≥ 2.1 V Input V_{out} ≥ 3.5 V dc coupled V_{out} ≥ 6.3 V square wave	3.0 5.0 9.0	— — —	0 0 0	— — —	0 0 0	— — —	0 0 0	V
V_{IH}	High–Level Input Voltage — f_{in}, OSC_{in}	V_{out} ≤ 0.9 V Input V_{out} ≤ 1.5 V dc coupled V_{out} ≤ 2.7 V square wave	3.0 5.0 9.0	3.0 5.0 9.0	— — —	3.0 5.0 9.0	— — —	3.0 5.0 9.0	— — —	V
V_{IL}	Low–Level Input Voltage — except f_{in}, OSC_{in}		3.0 5.0 9.0	— — —	0.9 1.5 2.7	— — —	0.9 1.5 2.7	— — —	0.9 1.5 2.7	V
V_{IH}	High–Level Input Voltage — except f_{in}, OSC_{in}		3.0 5.0 9.0	2.1 3.5 6.3	— — —	2.1 3.5 6.3	— — —	2.1 3.5 6.3	— — —	V
I_{in}	Input Current (f_{in}, OSC_{in})	V_{in} = V_{DD} or V_{SS}	9.0	±2.0	±50	±2.0	±25	±2.0	±22	µA
I_{IL}	Input Leakage Current (all inputs except f_{in}, OSC_{in})	V_{in} = V_{SS}	9.0	—	−0.3	—	−0.1	—	−1.0	µA
I_{IH}	Input Leakage Current (all inputs except f_{in}, OSC_{in})	V_{in} = V_{DD}	9.0	—	0.3	—	0.1	—	1.0	µA
C_{in}	Input Capacitance		—	—	10	—	10	—	10	pF
V_{OL}	Low–Level Output Voltage — OSC_{out}	I_{out} = 0 µA V_{in} = V_{DD}	3.0 5.0 9.0	— — —	0.9 1.5 2.7	— — —	0.9 1.5 2.7	— — —	0.9 1.5 2.7	V
V_{OH}	High–Level Output Voltage — OSC_{out}	I_{out} = 0 µA V_{in} = V_{SS}	3.0 5.0 9.0	2.1 3.5 6.3	— — —	2.1 3.5 6.3	— — —	2.1 3.5 6.3	— — —	V

(continued)

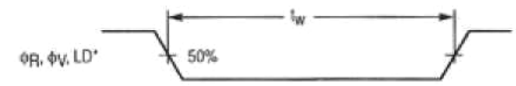
ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Conditions	V_{DD} V	−40°C Min	−40°C Max	25°C Min	25°C Max	85°C Min	85°C Max	Unit
V_{OL}	Low–Level Output Voltage — Other Outputs	$I_{out} \approx 0\ \mu A$	3.0 5.0 9.0	— — —	0.05 0.05 0.05	— — —	0.05 0.05 0.05	— — —	0.05 0.05 0.05	V
V_{OH}	High–Level Output Voltage — Other Outputs	$I_{out} \approx 0\ \mu A$	3.0 5.0 9.0	2.95 4.95 8.95	— — —	2.95 4.95 8.95	— — —	2.95 4.95 8.95	— — —	V
I_{OL}	Low–Level Sinking Current — Lock Detect	$V_{out} = 0.3$ V $V_{out} = 0.4$ V $V_{out} = 0.5$ V	3.0 5.0 9.0	0.25 0.64 1.3	— — —	0.2 0.51 1.0	— — —	0.15 0.36 0.7	— — —	mA
I_{OH}	High–Level Sourcing Current — Lock Detect	$V_{out} = 2.7$ V $V_{out} = 4.6$ V $V_{out} = 8.5$ V	3.0 5.0 9.0	−0.25 −0.64 −1.3	— — —	−0.2 −0.51 −1.0	— — —	−0.15 −0.36 −0.7	— — —	mA
I_{OL}	Low–Level Sinking Current — Other Outputs	$V_{out} = 0.3$ V $V_{out} = 0.4$ V $V_{out} = 0.5$ V	3.0 5.0 9.0	0.44 0.64 1.3	— — —	0.35 0.51 1.0	— — —	0.22 0.36 0.7	— — —	mA
I_{OH}	High–Level Sourcing Current — Other Outputs	$V_{out} = 2.7$ V $V_{out} = 4.6$ V $V_{out} = 8.5$ V	3.0 5.0 9.0	−0.44 −0.64 −1.3	— — —	−0.35 −0.51 −1.0	— — —	−0.22 −0.36 −0.7	— — —	mA
I_{OZ}	Output Leakage Current — PD_{out}	$V_{out} = V_{DD}$ or V_{SS} Output in Off State	9.0	—	± 0.3	—	± 0.1	—	± 1.0	µA
C_{out}	Output Capacitance — PD_{out}	PD_{out} — Three–State	—	—	10	—	10	—	10	pF

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 10 ns)

Symbol	Parameter	Figure No.	V_{DD} V	Guaranteed Limit 25°C	Guaranteed Limit −40 to 85°C	Unit
t_w	Output Pulse Width, ϕ_R, ϕ_V, and LD with f_R in Phase with f_V	1, 5	3.0 5.0 9.0	25 to 200 20 to 100 10 to 70	25 to 260 20 to 125 10 to 80	ns
t_{TLH}, t_{THL}	Maximum Output Transition Time, LD	2, 5	3.0 5.0 9.0	180 90 70	200 120 90	ns
t_{TLH}, t_{THL}	Maximum Output Transition Time, Other Outputs	2, 5	3.0 5.0 9.0	160 80 60	175 100 65	ns
t_{su}	Minimum Setup Time, Data to ST	3	3.0 5.0 9.0	10 10 10	— — —	ns
t_{su}	Minimum Setup Time, Address to ST	3	3.0 5.0 9.0	25 20 15	— — —	ns
t_h	Minimum Hold Time, Address to ST	3	3.0 5.0 9.0	10 10 10	— — —	ns
t_h	Minimum Hold Time, Data to ST	3	3.0 5.0 9.0	25 20 15	— — —	ns
t_w	Minimum Input Pulse Width, ST	4	3.0 5.0 9.0	40 30 20	— — —	ns

SWITCHING WAVEFORMS



* f_R in phase with f_V

Figure 1.

Figure 2.

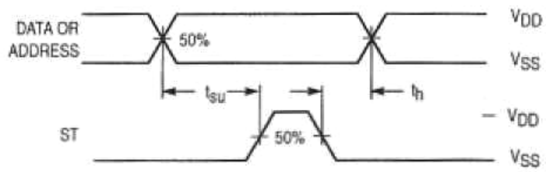


Figure 3.

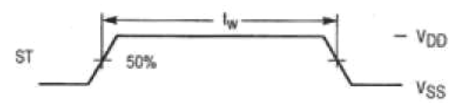
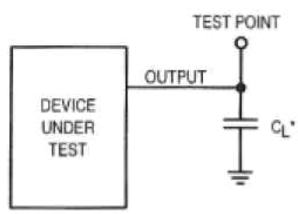


Figure 4.

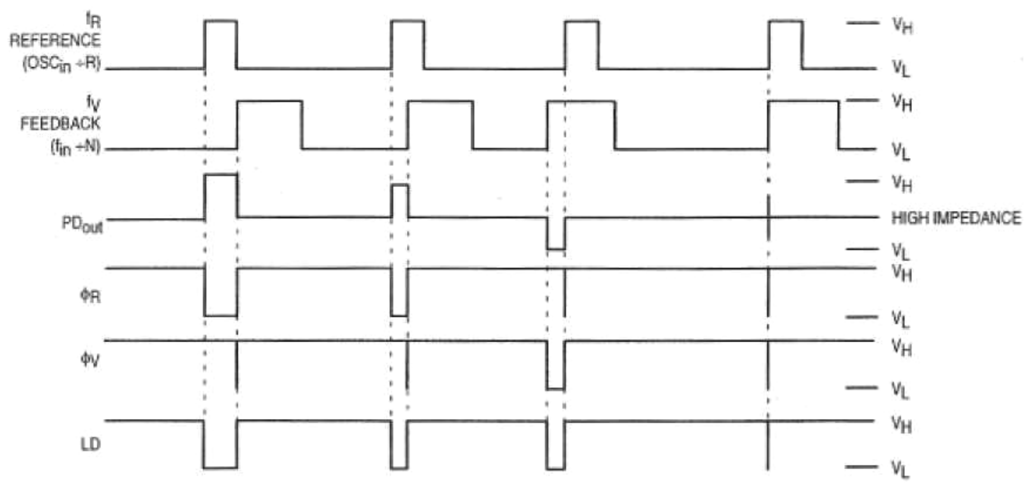


* Includes all probe and fixture capacitance.

Figure 5. Test Circuit

FREQUENCY CHARACTERISTICS (Voltages Referenced to V_{SS}, C_L = 50 pF, Input $t_r = t_f$ = 10 ns unless otherwise indicated)

Symbol	Parameter	Test Conditions	V_{DD} V	−40°C		25°C		85°C		Unit
				Min	Max	Min	Max	Min	Max	
f_i	Input Frequency (f_{in}, OSC_{in})	R ≥ 8, A ≥ 0, N ≥ 8 V_{in} = 500 mV p–p ac coupled sine wave	3.0 5.0 9.0	— — —	6.0 15 15	— — —	6.0 15 15	— — —	6.0 15 15	MHz
		R ≥ 8, A ≥ 0, N ≥ 8 V_{in} = 1.0 V p–p ac coupled sine wave	3.0 5.0 9.0	— — —	12 22 25	— — —	12 20 22	— — —	7.0 20 22	MHz
		R ≥ 8, A ≥ 0, N ≥ 8 V_{in} = V_{DD} to V_{SS} dc coupled square wave	3.0 5.0 9.0	— — —	13 25 25	— — —	12 22 25	— — —	8.0 22 25	MHz



V_H = High voltage level.
V_L = Low voltage level.
* At this point, when both f_R and f_V are in phase, the output is forced to near mid supply.
NOTE: The PD_{out} generates error pulses during out–of–lock conditions. When locked in phase and frequency, the output is high impedance and the voltage at that pin is determined by the low–pass filter capacitor.

Figure 6. Phase/Frequency Detectors and Lock Detector Output Waveforms

PIN DESCRIPTIONS

INPUT PINS

D0 – D3
Data Inputs (PDIP – Pins 2, 1, 18, 17; SOG – Pins 2, 1, 20, 19)

Information at these inputs is transferred to the internal latches when the ST input is in the high state. D3 is most signigicant bit.

f_{in}
Frequency Input (PDIP – Pin 3, SOG – Pin 4)

Input to ÷N portion of synthesizer. f_{in} is typically derived from the loop VCO and is ac couples. For larger amplitude signals (standard CMOS – logic levels) dc coupling may be used.

OSCin/OSCout
Reference Oscillator Input/Output (PDIP – Pins 6, 7; SOG – Pins 7, 8)

These pins form an on–chip reference oscillator when connected to terminals of an external parallel resonant crystal. Frequency setting capacitors of appropriate value must be connected from OSC_{in} to ground and OSC_{out} to ground. OSC_{in} may also serve as input for an externally–generated reference signal. This signal is typically AC coupled to OSC_{in} but for larger amplitude signals (standard CMOS–logic levels) DC coupling may also be used. In the external refrence mode, no connection is required to OSC_{out}.

A0 – A2
Address Inputs (PDIP – Pins 8, 9, 10; SOG – Pins 9, 10, 12)

A0, A1 and A2 are used to define which latch receives the information on the data input lines. The addresses refer to the following latches:

A2	A1	A0	Selected	Function	D0	D1	D2	D3
0	0	0	Latch 0	÷ N Bits	0	1	2	3
0	0	1	Latch 1	÷ N Bits	4	5	6	7
0	1	0	Latch 2	÷ N Bits	8	9	10	11
0	1	1	Latch 3	÷ N Bits	12	13	—	—
1	0	0	Latch 4	Reference Bits	0	1	2	3
1	0	1	Latch 5	Reference Bits	4	5	6	7
1	1	0	Latch 6	Reference Bits	8	9	10	11
1	1	1	—	—	—	—	—	—

ST
Strobe Transfer (PDIP – Pin 11, SOG – Pin 13)

The rising edge of strobe transfers data into the addressed latch, the falling edge of strobe latches data into the latch. This pin should normally be held low to avoid loading latches with invalid data.

OUTPUT PINS

PDout
Single–Ended Phase Detector output (PDIP – Pin 12, SOG – Pin 14)

Three–state output of phase detector for use as loop–error signal.

Frequency $f_V > f_R$ or f_V Leading: Negative Pulses
Frequency $f_V < f_R$ or f_V Lagging: Positive Pulses
Frequency $f_V = f_R$ and Phase Coincidence: High–Impedance State

LD
Lock Detector Signal (PDIP – Pin 13, SOG – Pin 15)

High level when loop is locked (f_R, f_V of same phase and frequency). Pulses low when loop is out of lock.

ϕV, ϕR
Phase Detect or Outputs (PDIP – Pin 12, SOG – Pin 14)

These phase detector outputs can be combined externally for a loop–error signal. A single–ended output is also available for this purpose (see PD_{out}).

If frequency f_V is greater than f_R or if the phase of f_V is leading, then error information is provided by ϕV pulsing low. ϕR remains essentially high.

If the frequency of f_V – f_R and both are in phase, then both ϕV and ϕR remain high except for a small minimum time period when both pulse low in phase.

REF_{out}
Buffered Reference Output (DIP – Pin 16, SOG – Pin 18)

Buffered output of on–chip reference oscillator or externally provided reference–input signal.

POWER SUPPLY PINS

V_{SS}
Ground (PDIP – Pin 4, SOG – Pin 5)

Circuit Ground

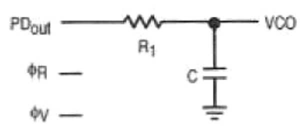
V_{DD}
Positive Power Supply (PDIP – Pin 5, SOG – Pin 6)

The positive supply voltage may range from 3.0 to 9.0 V with respect to V_{SS}.

DESIGN CONSIDERATIONS

PHASE–LOCKED LOOP — LOW–PASS FILTER DESIGN

A)

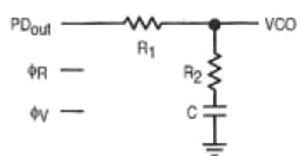


$$\omega_n = \sqrt{\frac{K_\phi K_{VCO}}{NR_1C}}$$

$$\zeta = \frac{N\omega_n}{2K_\phi K_{VCO}}$$

$$F(s) = \frac{1}{R_1sC + 1}$$

B)

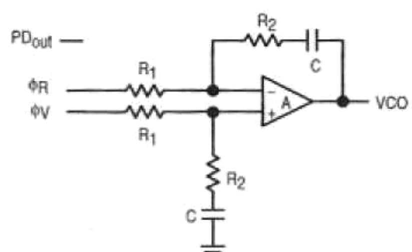


$$\omega_n = \sqrt{\frac{K_\phi K_{VCO}}{NC(R_1 + R_2)}}$$

$$\zeta = 0.5\,\omega_n\left(R_2C + \frac{N}{K_\phi K_{VCO}}\right)$$

$$F(s) = \frac{R_2sC + 1}{(R_1 + R_2)sC + 1}$$

C)



$$\omega_n = \sqrt{\frac{K_\phi K_{VCO}}{NCR_1}}$$

$$\zeta = \frac{\omega_n R_2C}{2}$$

ASSUMING GAIN A IS VERY LARGE, THEN:

$$F(s) = \frac{R_2sC + 1}{R_1sC}$$

NOTE: Sometimes R_1 is split into two series resistors, each $R_1 \div 2$. A capacitor C_C is then placed from the midpoint to ground to further filter ϕ_V and ϕ_R. The value of C_C should be such that the corner frequency of this network does not significantly affect ω_n.

DEFINITIONS:

N = Total Division Ratio in feedback loop

K_ϕ (Phase Detector Gain) = $V_{DD}/4\pi$ for PD_{out}

K_ϕ (Phase Detector Gain) = $V_{DD}/2\pi$ for ϕ_V and ϕ_R

K_{VCO} (VCO Gain) = $\dfrac{2\pi\Delta f_{VCO}}{\Delta V_{VCO}}$

for a typical design w_n (Natural Frequency) $\approx \dfrac{2\pi fr}{10}$ (at phase detector input).

Damping Factor: $\zeta \cong 1$

CRYSTAL OSCILLATOR CONSIDERATIONS

The following options may be considered to provide a reference frequency to Motorola's CMOS frequency sytnthesizers.

Use of a Hybrid Crystal Oscillator

Commercially available temperature–compensated crystal oscillators (TCXOs) or crystal–controlled data clock oscillators provide very stable reference frequencies. An oscillator capable of sinking and sourcing 50 μA at CMOS logic levels may be direct or DC coupled to OSC_{in}. In general, the highest frequency capability is obtained utilizing a direct–coupled square wave having a rail–to–rail (V_{DD} to V_{SS}) voltage swing. If the oscillator does not have CMOS logic levels on the outputs, capacitive or AC coupling to OSC_{in} may be used. OSC_{out}, and unbuffered output, should be left floating.

For additional information about TCXOs and data clock oscillators, please consult the latest version of the *eem Electronic Engineers Master Catalog*, the *Gold Book*, or similar publications.

Design an Off–Chip Reference

The user may design an off–chip crystal oscillator using ICs specifically developed for crystal oscillator applications, such as the ML12061 MECL device. The reference signal from the MECL device is ac coupled to OSC_{in}. For large amplitude signals (standard CMOS logic levels), DC coupling is used. OSC_{out}, an unbuffered output, should be left floating. In general, the highest freqency capability is obtained with a direct–coupled square wave having rail–to–rail voltage swing.

Use of the On–Chip Oscillator Circuitry

The on–chip amplifier (a digital inverter) along with an appropriate crystal may be used to provide a reference source frequency. A fundamental mode crystal, parallel resonant at the desired operating frequency, should be connected as shown in Figure 7.

For V_{DD} = 5.0 V, the crystal should be specified for a loading capacitanc. C_L, which does not exceed 32 pf for frequencies to approximately 8.0 to 15 MHz and 10 pF for higher frequencies. These are guidelines that provide a reasonable compromise between IC capacitance, drive capability, swamping c–variations in stray and IC input/output capacitance, and realistic C_L values. The shunt load capacitance. C_L, presented across the crystal can be estimated to be:

$$C_L = \frac{C_{in}C_{out}}{C_{in} + C_{out}} + C_a + C_o + \frac{C1 \cdot C2}{C1 + C2}$$

where

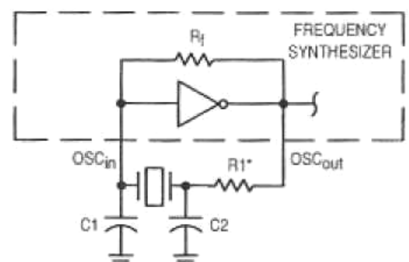
Cin = 5.0 pf (see Figure 8)
Cout = 6.0 pf (see Figure 8)
Ca = 1.0 pf (see Figure 8)
CO = the crystal's holder capacitance (see Figure 9)
C1 and C2 = external capacitors (see Figure 7)

The oscillator can be "trimmed" on–frequency by making a portion of all of C1 variable. The crystal and associated components must be located as close as possible to the OSC_{in} and OSC_{out} pins to minimize distortion, stray capacitance, stray inductance and startup stablilization time. In some cases, stray capacitance should be added to the value for C_{in} and C_{out}.

Power is dissipated in the effective series resistance of the crystal R_e, in Figure 9. The drive level specified by the crystal manufacturer is the maximum stress that a crystal can withstand without damage or excessive shift in frequency. R1 in Figure 7 limits the drive level. The use of R1 may not be necessary in some cases (i.e., R1 = 0 Ω)

To verify that the maximum dc supply voltage does not overdrive the crystal, monitor the output frequency as a function of voltage at OSC_{out}. (Care should be taken to minimize loading.) The frequency should increase very slightly as the dc supply voltage is increased. An overdriven crystal will decrease in frequency or become unstable with an increase in supply voltage. The operating supply voltage must be reduced or R1 must be increased in value if the overdriven condition exists. The user should note that the oscillator start–up time is proportional to the value of R1.

Through the process of supplying crystals for use with CMOS inverters, many crystal manufactureres have developed expertise in CMOS oscillator design with crystals. Discussions with such manufacturers can prove very helpful (see Table 1).



* May be deleted in certain cases. See text.

Figure 7. Pierce Crystal Oscillator Circuit

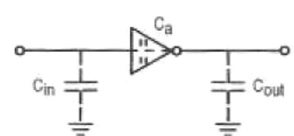
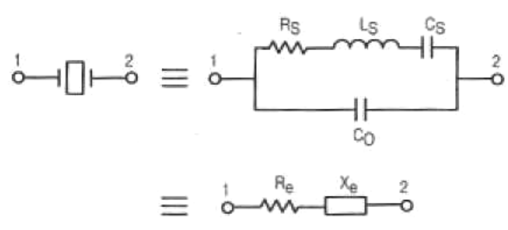


Figure 8. Parasitic Capacitances of the Amplifier



NOTE: Values are supplied by crystal manufacturer (parallel resonant crystal).

Figure 9. Equivalent Crystal Networks

Table 1. Partial List of Crystal Manufacturers

Name	Address	Phone
United States Crystal Corp.	3605 McCart Ave., Ft. Worth, TX 76110	(817) 921–3013
Crystek Crystal	2351 Crystal Dr., Ft. Myers, FL 33907	(813) 936–2109
Statek Corp.	512 N. Main St., Orange, CA 92668	(714) 639–7810

NOTE: Lansdale cannot recommend one supplier over another and in no way suggests that this is a complete listing of crystal manufacturers.

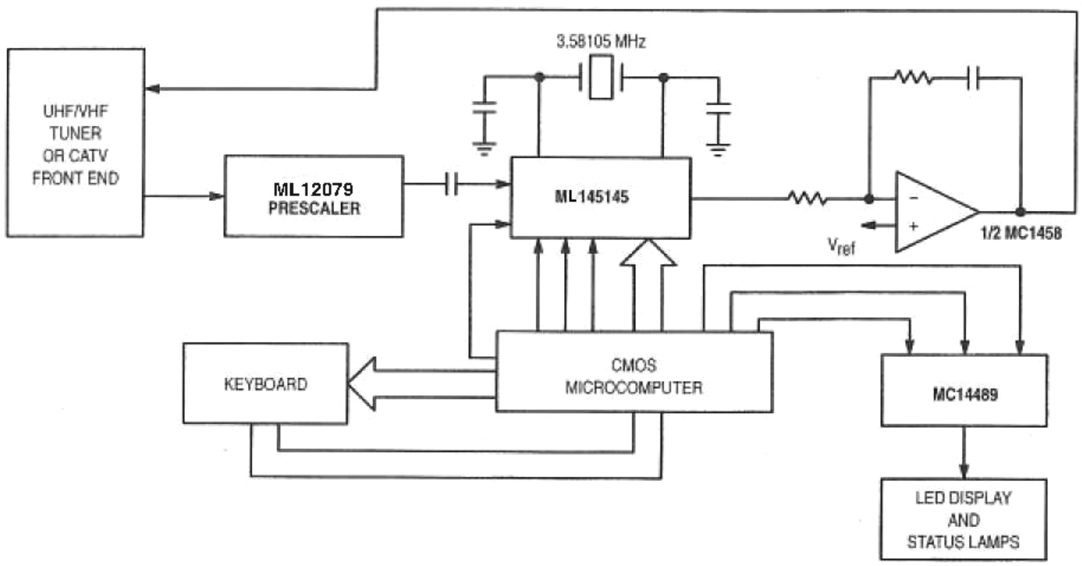


Figure 10. TV/CATV Tuning System

RECOMMENDED READING

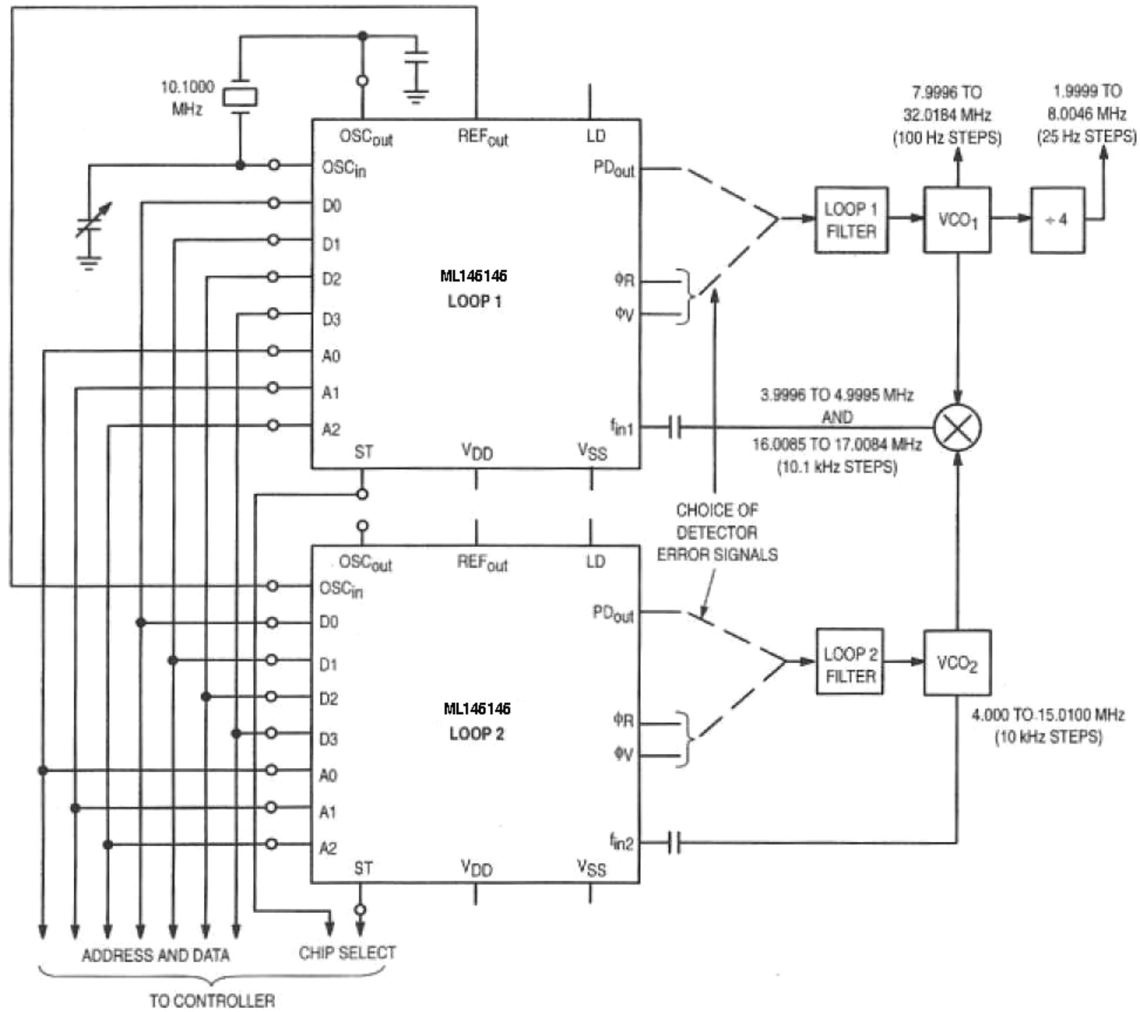
Technical Note TN–24, Stated Corp.
Technical Note TN–\7, Stated Corp.
E. Hafner, "The Piezoelectric Crystal Unit – Definitions and Method of Measurement", *Proc IEEE*, Vol. 57, No. 2 Feb., 1969
D. Kemper, L. Rosine, "Quartz Crystals for Frequency Control", *Electro–Technology*, June, 1969.
P.J. Ottowitz, "A Guide to Crystal Selection", *Electronic Design*, May, 1966.

LEGACY APPLICATIONS

The features of the ML145145 permit bus operation with a dedicated wire needed only for the strobe input. In a microprocessor–controlled system this strobe input is accessed when the PLL is addressed. The remaining data and address inputs will directly interface to the microprocessor's data and address buses.

The ÷ R programability is used to advantage in Figure 10. Here, the nominal ÷ R value is 3667, but by programming small changes in this value, fine tuning is accomplised. Better tuning resolution is achievable with this method than by changing the ÷ N due to the use of the large fixed prescaling value of ÷ 256 provided by the ML12079.

The two–loop synthesizer, in Figure 11, takes advantage of these features to control the phase–locked loop with a minumum of dedicated lines while preserving optimal loop performance. Both 25 Hz and 100 Hz steps are provided while the relatively large reference frequencies of 10 Khz or 10.1 kHz are maintained.



NOTES:
1. Table 2 provides program sequence for the ÷ N1 (Loop 1) and ÷ N2 (Loop 2) Counters.
2. ÷ R1 = 1000, f_{R1} = 10.1 kHz, ÷ R2 = 1010, f_{R2} = 10 kHz.
3. $f_{VCO1} = N1(f_{R1}) + N2(f_{R2}) = N1(f_{R2} + \Delta f) + N2(f_{R2})$ where Δf = 100 Hz.
4. Other f_{R1} and f_{R2} values may be used with appropriate ÷ N1 and ÷ N2 changes.

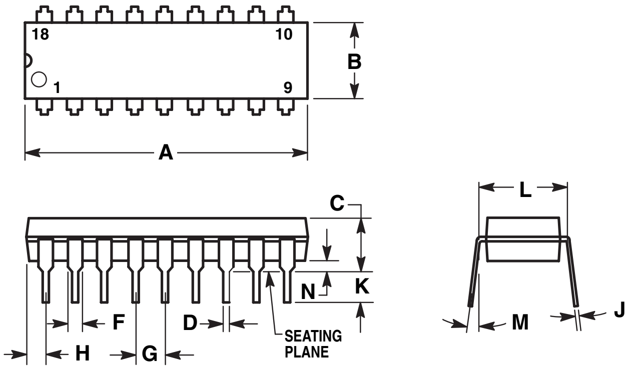
Figure 11. Two–Loop Synthesizer Provides 25 and 100 Hz Frequency Steps While Maintaining High Detector Comparison Frequencies of 10 and 10.1 kHz

Table 2. Programming Sequence for Two–Loop Synthesizer of Figure 11

÷ N1	f_{in1} (MHz)	÷ N2	f_{VCO2} (MHz)	f_{VCO1} (MHz)
"A" 396 397 ↓ 495	"B" 3.9996 4.0097 ↓ 4.9995	400 399 ↓ 301	4.0000 3.9900 ↓ 3.0100	7.9996 7.9997 ↓ 8.0095
"A"	"B"	401 400 ↓ 303	4.0100 4.0000 ↓ 3.0200	8.0096 8.0097 ↓ 8.0195
"A"	"B"	"C" 402 401 ↓ 303	"D" 4.0200 4.0100 ↓ 3.0300	8.0196 8.0197 ↓ 8.0295
"A"	"B"	↓ 1500	↓ 15.0000	Increasing In 100 Hz Steps ↓ 19.9995
"A"	"B"	1600 1599 ↓ 1501	16.0000 15.9900 ↓ 15.0100	19.9996 19.9997 ↓ 20.0095
"E" 1585 1586 ↓ 1684	"F" 16.0085 16.0186 ↓ 17.0084			20.0085 20.0086 ↓ 20.0184
"E"	"F"	"C"	"D"	20.0185 20.0186 ↓ 20.0284
				Increasing In 100 Hz Steps ↓ 32.0084
"E"	"F"			32.0085 32.0086 ↓ 32.0184

OUTLINE DIMENSIONS

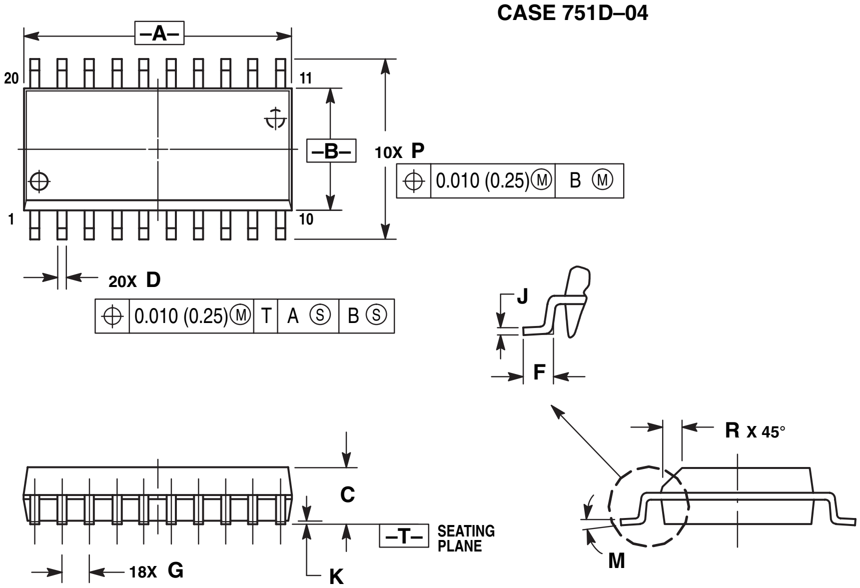
P DIP 18 = VP (ML145145VP) CASE 707–02



NOTES:
1. POSITIONAL TOLERANCE OF LEADS (D), SHALL BE WITHIN 0.25 (0.010) AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	22.22	23.24	0.875	0.915
B	6.10	6.60	0.240	0.260
C	3.56	4.57	0.140	0.180
D	0.36	0.56	0.014	0.022
F	1.27	1.78	0.050	0.070
G	2.54 BSC		0.100 BSC	
H	1.02	1.52	0.040	0.060
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	7.62 BSC		0.300 BSC	
M	0°	15°	0°	15°
N	0.51	1.02	0.020	0.040

SOG 20W = -6P (ML145145-6P) CASE 751D–04



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.150 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOW ABLE DAMBAR PROTRUSION SHALL BE 0.13 (0.005) TOTAL IN EXCESS OF D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	12.65	12.95	0.499	0.510
B	7.40	7.60	0.292	0.299
C	2.35	2.65	0.093	0.104
D	0.35	0.49	0.014	0.019
F	0.50	0.90	0.020	0.035
G	1.27 BSC		0.050 BSC	
J	0.25	0.32	0.010	0.012
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	10.05	10.55	0.395	0.415
R	0.25	0.75	0.010	0.029