MOTOROLA

MC145145-1

Advance Information

4-BIT DATA BUS INPUT PLL FREQUENCY SYNTHESIZER

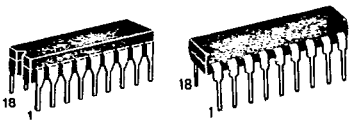
The MC145145-1 is programmed by a 4-bit input, with strobe and address lines. The device features consist of a reference oscillator, 12-bit programmable reference divider, digital-phase detector, 14-bit programmable divide-by-N counter and the necessary latch circuitry for accepting the 4-bit input data. When combined with a loop filter and VCO, the MC145145-1 can provide all the remaining functions for a PLL frequency synthesizer operating up to the device's frequency limit. For higher VCO frequency operation, a down mixer or a fixed divide prescaler can be used between the VCO and MC145145-1.

The MC145145-1 offers improved performance over the MC145145. The ac characteristics have been improved and the input current requirements have been modified.

- General Purpose Applications:
  - CATV
  - TV Tuning
  - AM/FM Radios
  - Scanning Receivers
  - Two Way Radios
  - Amateur Radio
- Low Power Consumption
- 3.0 to 9.0 V Supply Range
- On- or Off-Chip Reference Oscillator Operation
- Single Modulus 4-Bit Data Bus Programming
- ÷ R Range = 3 to 4095
- ÷ N Range = 3 to 16383
- "Linearized" Digital Phase Detector Enhances Transfer Function Linearity
- Two Error Signal Options:
  - Single Ended (Three State)
  - Double Ended

HIGH-PERFORMANCE
CMOS
LOW-POWER COMPLEMENTARY MOS
SILICON-GATE

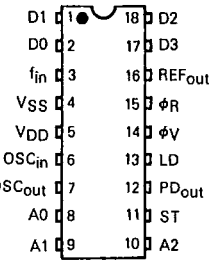
4-BIT DATA BUS INPUT PLL FREQUENCY SYNTHESIZER



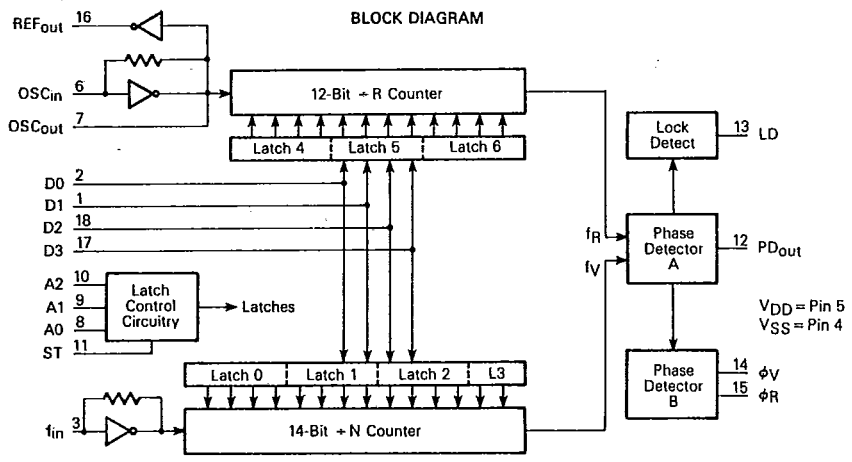
MC145145L1
CERAMIC PACKAGE
CASE 726

MC145145P1
PLASTIC PACKAGE
CASE 707

PIN ASSIGNMENT



BLOCK DIAGRAM



This document contains information on a new product. Specifications and information herein are subject to change without notice.

MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	−0.5 to +10	V
V_{in}, V_{out}	Input or Output Voltage (DC or Transient)	−0.5 to V_{DD}+0.5	V
I_{in}, I_{out}	Input or Output Current (DC or Transient), per Pin	±10	mA
I_{DD}, I_{SS}	Supply Current, V_{DD} or V_{SS} Pins	±30	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	−65 to +150	°C
T_L	Lead Temperature (8-Second Soldering)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.

†Power Dissipation Temperature Derating:
Plastic "P" Package: −12 mW/°C from 65°C to 85°C
Ceramic "L" Package: No derating

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

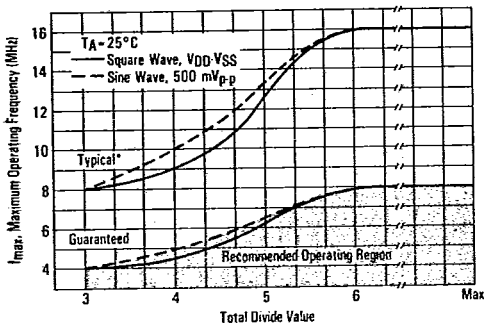
Characteristic	Symbol	V_{DD}	−40°C Min	−40°C Max	25°C Min	25°C Typ	25°C Max	85°C Min	85°C Max	Units
Power Supply Voltage Range	V_{DD}	–	3	9	3	–	9	3	9	V
Output Voltage 0 Level V_{in}=0 V or V_{DD} I_{out}≈0 μA	V_{OL}	3	–	0.05	–	0.001	0.05	–	0.05	V
		5	–	0.05	–	0.001	0.05	–	0.05	
		9	–	0.05	–	0.001	0.05	–	0.05	
1 Level	V_{OH}	3	2.95	–	2.95	2.999	–	2.95	–	
		5	4.95	–	4.95	4.999	–	4.95	–	
		9	8.95	–	8.95	8.999	–	8.95	–	
Input Voltage 0 Level V_{out}=0.5 V or V_{DD}−0.5 V (All Outputs Except OSC_{out})	V_{IL}	3	–	0.9	–	1.35	0.9	–	0.9	V
		5	–	1.5	–	2.25	1.5	–	1.5	
		9	–	2.7	–	4.05	2.7	–	2.7	
1 Level	V_{IH}	3	2.1	–	2.1	1.65	–	2.1	–	
		5	3.5	–	3.5	2.75	–	3.5	–	
		9	6.3	–	6.3	4.95	–	6.3	–	
Output Current	I_{OH}									mA
V_{out}=2.7 V Source		3	−0.44	–	−0.35	−1.0	–	−0.22	–	
V_{out}=4.6 V		5	−0.64	–	−0.51	−1.2	–	−0.36	–	
V_{out}=8.5 V		9	−1.30	–	−1.00	−2.0	–	−0.70	–	
V_{out}=0.3 V Sink	I_{OL}	3	0.44	–	0.35	1.0	–	0.22	–	
V_{out}=0.4 V		5	0.64	–	0.51	1.2	–	0.36	–	
V_{out}=0.5 V		9	1.30	–	1.00	2.0	–	0.70	–	
Input Current — Other Inputs	I_{in}	9	–	±0.3	–	±0.00001	±0.1	–	±1.0	μA
Input Current — f_{in}, OSC_{in}	I_{in}	9	–	±50	–	±10	±25	–	±22	μA
Input Capacitance	C_{in}	–	–	10	–	6	10	–	10	pF
3-State Output Capacitance — PD_{out}	C_{out}	–	–	10	–	6	10	–	10	pF
Quiescent Current V_{in}=0 V or V_{DD} I_{out}=0 μA	I_{DD}	3	–	800	–	200	800	–	1600	μA
		5	–	1200	–	300	1200	–	2400	
		9	–	1600	–	400	1600	–	3200	
3-State Leakage Current — PD_{out} V_{out}=0 V or 9 V	I_{OZ}	9	–	±0.3	–	±0.0001	±0.1	–	±3.0	μA

SWITCHING CHARACTERISTICS ($T_A = 25°C$, $C_L = 50$ pF)

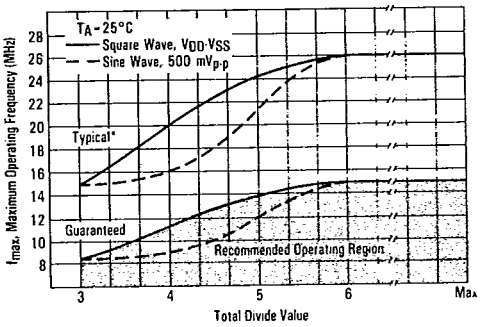
Characteristic	Symbol	V_{DD}	Min	Typ	Max	Units
Output Rise and Fall Time (Figures 1 and 6)	t_{TLH}, t_{THL}	3	–	60	140	ns
		5	–	40	80	
		9	–	30	60	
Setup Times	t_{su}	3	10	0	–	ns
Data to ST (Figure 2)		5	10	0	–	
		9	10	0	–	
Address to ST (Figure 2)		3	80	60	–	
		5	50	30	–	
		9	30	18	–	
Hold Times	t_h	3	25	10	–	ns
Data to Strobe (Figure 2)		5	20	10	–	
		9	15	10	–	
Address to Strobe (Figure 2)		3	35	15	–	
		5	25	10	–	
		9	20	10	–	
Output Pulse Width	$t_{w\phi}$	3	25	100	175	ns
ϕ_R, ϕ_V with f_R in		5	20	60	100	
Phase with f_V (Figures 3 and 6)		9	10	40	70	
Input Rise and Fall Times	t_r, t_f	3	–	20	5	μs
OSC_{in}, f_{in} (Figure 4)		5	–	5	2	
		9	–	2	0.5	
Input Pulse Width	t_w	3	40	30	–	ns
ST (Figure 5)		5	35	20	–	
		9	25	15	–	

GRAPH 1 — OSC_{in} AND f_{in} MAXIMUM FREQUENCY VERSUS TOTAL DIVIDE VALUE

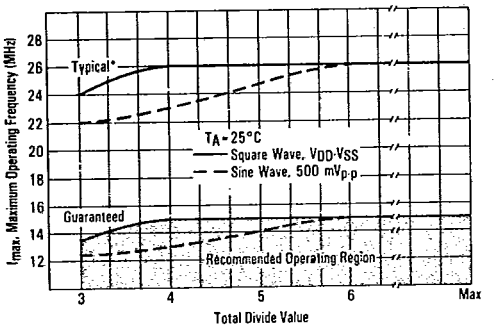
GRAPH 1A — V_{DD} = 3 V



GRAPH 1B — V_{DD} = 5 V

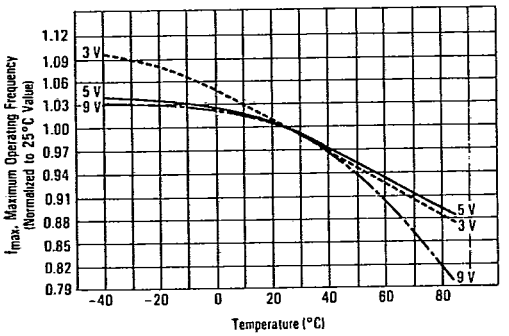


GRAPH 1C — V_{DD} = 9 V

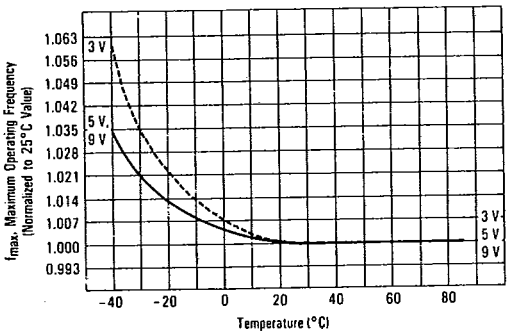


GRAPH 2 — OSC_{in} AND f_{in} MAXIMUM FREQUENCY VERSUS TEMPERATURE FOR SINE AND SQUARE WAVE INPUTS

GRAPH 2A — TOTAL DIVIDE VALUE = 3, 4, OR 5



GRAPH 2B — TOTAL DIVIDE VALUE ≥ 6



*Data labelled "Typical" is not to be used for design purposes, but is intended as an indication of the IC's potential performance.

PIN DESCRIPTIONS

DATA INPUTS (Pins 2, 1, 18, 17) — Information at these inputs is transferred to the internal latches when the ST input is in the high state. Pin 17 (D3) is most significant.

f_{in} (Pin 3) — Input to ÷N portion of synthesizer. f_{in} is typically derived from loop VCO and is AC coupled into Pin 3. For larger amplitude signals (standard CMOS-logic levels) DC coupling may be used.

V_{SS} (Pin 4) — Circuit Ground.

V_{DD} (Pin 5) — Positive power supply.

OSC_{in}, OSC_{out} (Pins 6 and 7) — These pins form an on-chip reference oscillator when connected to terminals of an external parallel resonant crystal. Frequency setting capacitors of appropriate value must be connected from OSC_{in} to ground and OSC_{out} to ground. OSC_{in} may also serve as input for an externally-generated reference signal. This signal will typically be AC coupled to OSC_{in}, but for larger amplitude signals (standard CMOS-logic levels) DC coupling may also be used. In the external reference mode, no connection is required to OSC_{out}.

ADDRESS INPUTS (Pins 8, 9, 10) — A0, A1 and A2 are used to define which latch receives the information on the data input lines. The addresses refer to the following latches:

A2	A1	A0	Selected	Function	D0	D1	D2	D3
0	0	0	Latch 0	÷N Bits	0	1	2	3
0	0	1	Latch 1	÷N Bits	4	5	6	7
0	1	0	Latch 2	÷N Bits	8	9	10	11
0	1	1	Latch 3	÷N Bits	12	13	—	—
1	0	0	Latch 4	Reference Bits	0	1	2	3
1	0	1	Latch 5	Reference Bits	4	5	6	7
1	1	0	Latch 6	Reference Bits	8	9	10	11
1	1	1	—	—	—	—	—	—

ST (Pin 11) — When high, this input will enter the data that appears at the D0, D1, D2 and D3 inputs, and when low, will latch that information. When high, any changes in the data information will be transferred into the latches.

PD_{out} (Pin 12) — Three-state output of phase detector for use as loop error signal.

Frequency $f_V > f_R$ or f_V Leading: Negative Pulses.
Frequency $f_V < f_R$ or f_V Lagging: Positive Pulses.
Frequency $f_V = f_R$ and Phase Coincidence: High-Impedance State.

LD (Pin 13) — Lock detector signal. High level when loop is locked (f_R, f_V of same phase and frequency). Pulses low when loop is out of lock.

ϕV, ϕR (Pins 14 and 15) — These phase detector outputs can be combined externally for a loop error signal. A single-ended output is also available for this purpose (see PD_{out}).

If frequency f_V is greater than f_R or if the phase of f_V is leading, then error information is provided by ϕV pulsing low. ϕR remains essentially high.

If the frquency f_V is less than f_R or if the phase of f_V is lagging, then error information is provided by ϕR pulsing low. ϕV remains essentially high.

If the frequency of $f_V = f_R$ and both are in phase, then both ϕV and ϕR remain high except for a small minimum time period when both pulse low in phase.

REF_{out} (Pin 16) — Buffered output of on-chip reference oscillator or externally provided reference-input signal.

SWITCHING WAVEFORMS

FIGURE 1

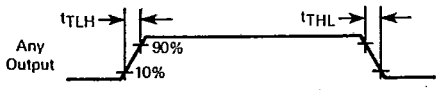


FIGURE 2

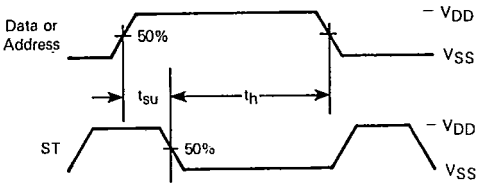
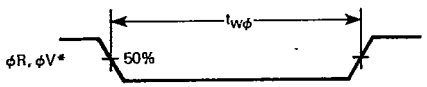


FIGURE 3



* f_r in phase with f_v

FIGURE 4

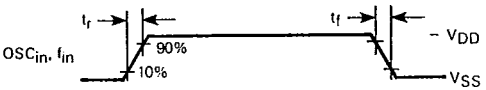


FIGURE 5

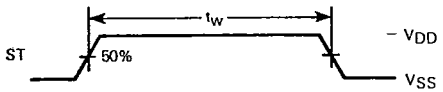
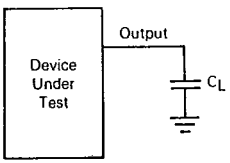
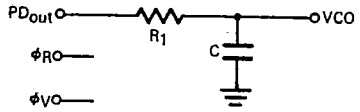


FIGURE 6 — TEST CIRCUIT



PHASE LOCKED LOOP — LOW PASS FILTER DESIGN

A)

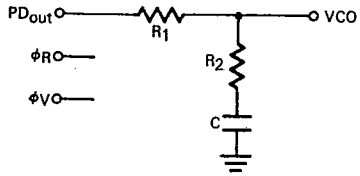


$$\omega_n = \sqrt{\frac{K_\phi K_{VCO}}{NR_1C}}$$

$$\zeta = \frac{N\omega_n}{2K_\phi K_{VCO}}$$

$$F(s) = \frac{1}{R_1CS + 1}$$

B)

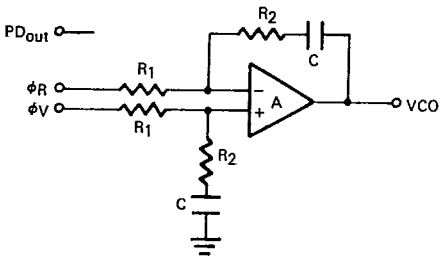


$$\omega_n = \sqrt{\frac{K_\phi K_{VCO}}{NC(R_1 + R_2)}}$$

$$\zeta = 0.5\omega_n\left(R_2C + \frac{N}{K_\phi K_{VCO}}\right)$$

$$F(s) = \frac{R_2CS + 1}{S(R_1C + R_2C) + 1}$$

C)



$$\omega_n = \sqrt{\frac{K_\phi K_{VCO}}{NCR_1}}$$

$$\zeta = \frac{\omega_n R_2 C}{2}$$

Assuming gain A is very large, then:

$$F(s) = \frac{R_2CS + 1}{R_1CS}$$

NOTE: Sometimes R_1 is split into two series resistors each $R_1 \div 2$. A capacitor C_C is then placed from the midpoint to ground to further filter ϕ_V and ϕ_R. The value of C_C should be such that the corner frequency of this network does not significantly affect ω_n.

DEFINITIONS: N = Total Division Ratio in feedback loop

$K_\phi = V_{DD}/4\pi$ for PD_{out}

$K_\phi = V_{DD}/2\pi$ for ϕ_V and ϕ_R

$$K_{VCO} = \frac{2\pi\Delta f_{VCO}}{\Delta V_{VCO}}$$

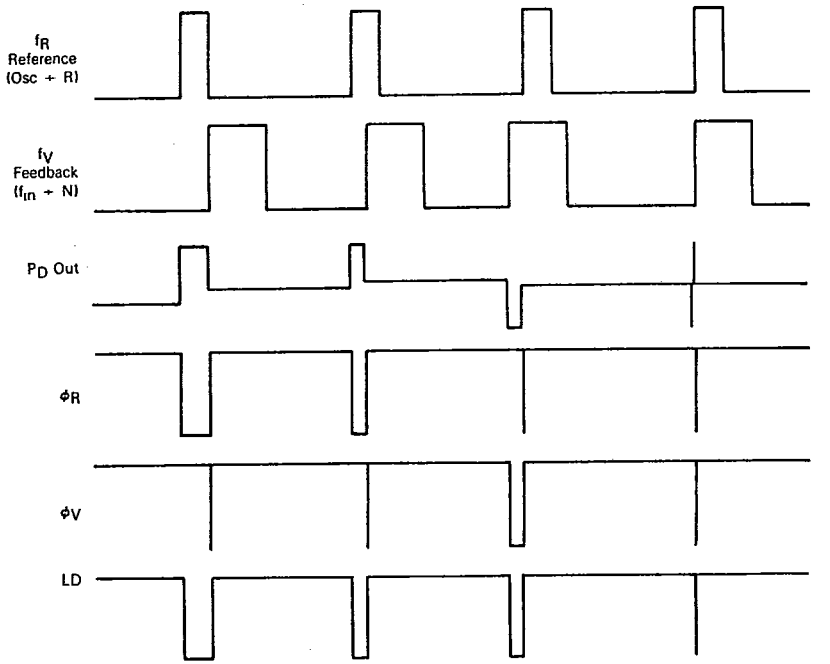
for a typical design $\omega_n \cong \frac{2\pi f_r}{10}$ (at phase detector input),

$$\zeta \cong 1$$

RECOMMENDED FOR READING:

Gardner, Floyd M., *Phaselock Techniques (second edition)*. New York, Wiley-Interscience, 1979.
Manassewitsch, Vadim, *Frequency Synthesizers: Theory and Design (second edition)*. New York, Wiley-Interscience, 1980.
Blanchard, Alain, *Phase-Locked Loops: Application to Coherent Receiver Design*. New York, Wiley-Interscience, 1976.
Egan, William F., *Frequency Synthesis by Phase Lock*. New York, Wiley-Interscience, 1981.
Rohde, Ulrich L., *Digital PLL Frequency Synthesizers Theory and Design*. Englewood Cliffs, NJ, Prentice-Hall, 1983.
Berlin, Howard M., *Design of Phase-Locked Loop Circuits, with Experiments*. Indianapolis, Howard W. Sams and Co., 1978.
Kinley, Harold, *The PLL Synthesizer Cookbook*. Blue Ridge Summit, PA, Tab Books, 1980.

FIGURE 7 — PHASE DETECTOR OUTPUT WAVEFORMS



NOTE: The P_D output state is equal to either V_{DD} or V_{SS} when active. When not active, the output is high impedance and the voltage at that pin is determined by the low pass filter capacitor.

APPLICATIONS

The features of the MC145145-1 permit bus operation with a dedicated wire needed only for the strobe input. In a microprocessor-controlled system this strobe input is accessed when the phase lock loop is addressed. The remaining data and address inputs will directly interface to the microprocessor's data and address buses.

The ÷ R programmability is used to advantage in Figure 8. Here, the nominal ÷ R value is 3667; but by programming small changes in this value, fine tuning is accomplished. Better tuning resolution is achievable with this method than by changing the ÷ N, due to the use of the large fixed prescaling value of ÷ 256 provided by the MC12071.

The two loop synthesizer, in Figure 9, takes advantage of these features to control the phase locked loop with a minimum of dedicated lines while preserving optimal loop performance. Both 25 Hz and 100 Hz steps are provided while the relatively large reference frequencies of 10 kHz or 10.1 kHz are maintained.

FIGURE 8 — TV/CATV TUNING SYSTEM

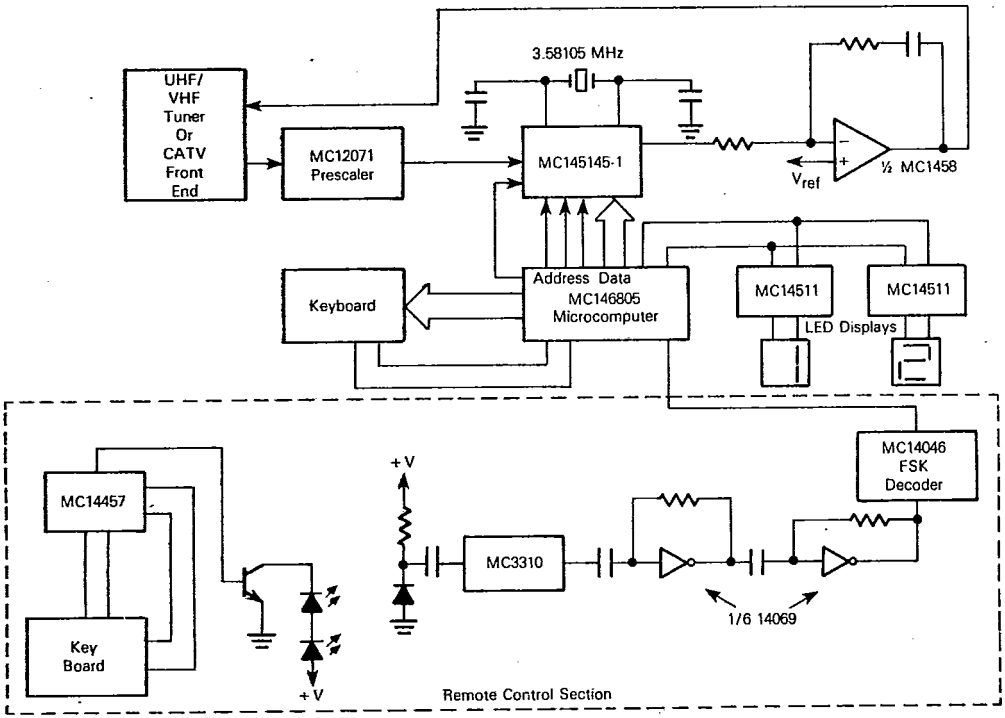
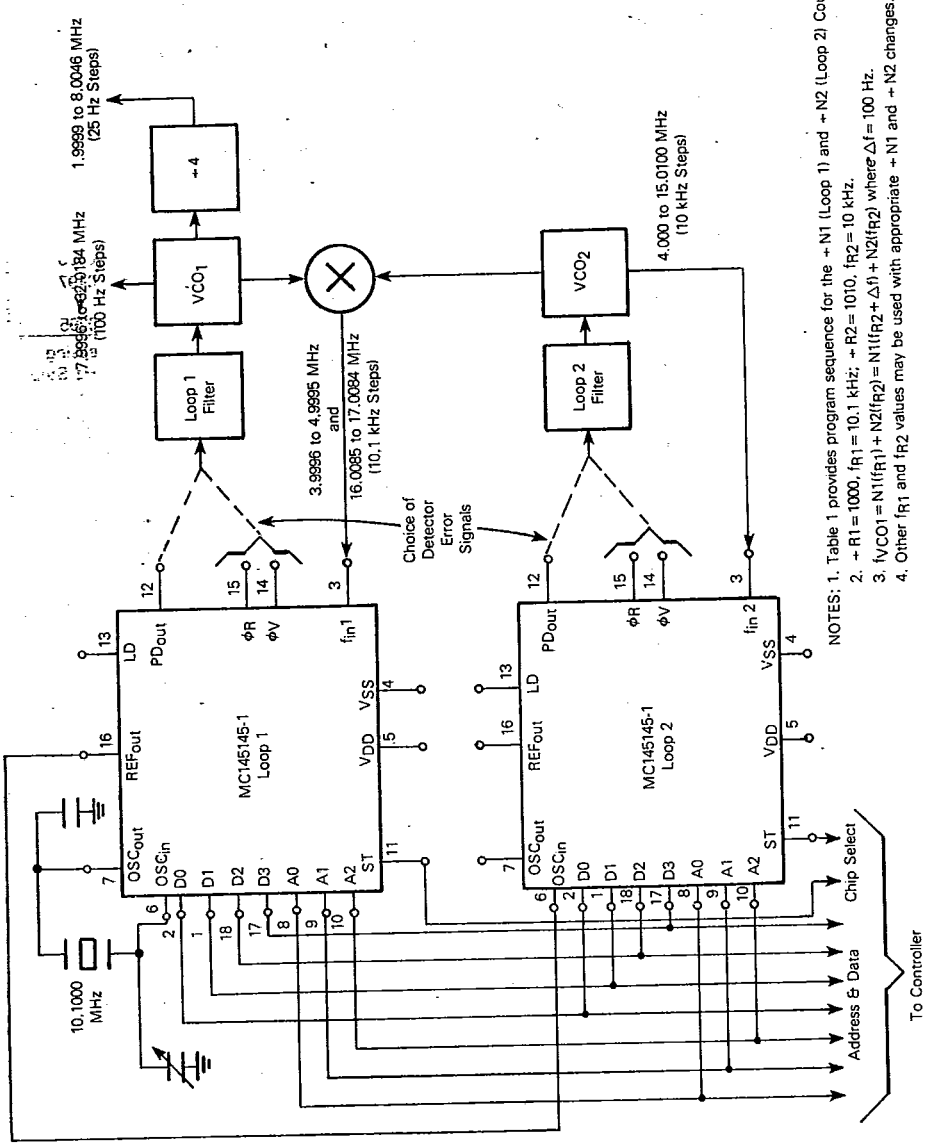


FIGURE 9 — TWO-LOOP SYNTHESIZER PROVIDES 25 AND 100 Hz FREQUENCY STEPS WHILE MAINTAINING HIGH DETECTOR COMPARISON FREQUENCIES OF 10 AND 10.1 kHz



NOTES: 1. Table 1 provides program sequence for the ÷N1 (Loop 1) and ÷N2 (Loop 2) Counters.
2. ÷R1 = 1000, f_{R1} = 10.1 kHz; ÷R2 = 1010, f_{R2} = 10 kHz.
3. $f_{VCO1} = N1(f_{R1}) + N2(f_{R2}) = N1(f_{R2} + \Delta f) + N2(f_{R2})$ where Δf = 100 Hz.
4. Other f_{R1} and f_{R2} values may be used with appropriate ÷N1 and ÷N2 changes.

TABLE 1 — PROGRAMMING SEQUENCE FOR TWO-LOOP SYNTHESIZER OF FIGURE 9

÷N1	f_{in1} (MHz)	÷N2	f_{VCO2} (MHz)	f_{VCO1} (MHz)
396 "A" 397 495	3.9996 "B" 4.0097 4.9995	400 399 301	4.0000 3.9900 3.0100	7.9996 7.9997 8.0095
"A"	"B"	401 400 302	4.0100 4.0000 3.0200	8.0096 8.0097 8.0195
"A"	"B"	402 "C" 401 303	4.0200 "D" 4.0100 3.0300	8.0196 8.0197 8.0295
		1500	15.0000	Increasing In 100 Hz Steps 19.9995
"A"	"B"	1600 1599 1501	16.0000 15.9900 15.0100	19.9996 19.9997 20.0095
1585 "E" 1586 1684	16.0085 "F" 16.0186 17.0084			20.0085 20.0086 20.0184
"E"	"F"	"C"	"D"	20.0185 20.0186 20.0284
				Increasing In 100 Hz Steps 32.0084
"E"	"F"			32.0085 32.0086 32.0184

CRYSTAL OSCILLATOR CONSIDERATIONS

The following options may be considered to provide a reference frequency to Motorola's CMOS frequency synthesizers. The most desirable is discussed first.

USE OF A HYBRID CRYSTAL OSCILLATOR

Commercially available temperature-compensated crystal oscillators (TXCOs) or crystal-controlled data clock oscillators provide very stable reference frequencies. An oscillator capable of sinking and sourcing 50 μA at CMOS logic levels may be direct or dc coupled to OSC_{in}. In general, the highest frequency capability is obtained utilizing a direct-coupled square wave having a rail-to-rail (V_{DD} to V_{SS}) voltage swing. If the oscillator does not have CMOS logic levels on the outputs, capacitive or ac coupling to OSC_{in} may be used. OSC_{out}, an unbuffered output, should be left floating.

For additional information about TXCOs and data clock oscillators, please contact: Motorola Inc., Component Products, 2553 N. Edgington St., Franklin Park, IL 60131, phone (312) 451-1000.

DESIGN AN OFF-CHIP REFERENCE

The user may design an off-chip crystal oscillator using ICs specifically developed for crystal oscillator applications, such as the MC12060, MC12061, MC12560, or MC12561 MECL devices. The reference signal from the MECL device is ac coupled to OSC_{in}. For large amplitude signals (standard CMOS logic levels), dc coupling is used. OSC_{out}, an unbuffered output, should be left floating. In general, the highest frequency capability is obtained with a direct-coupled square wave having rail-to-rail voltage swing.

USE OF THE ON-CHIP OSCILLATOR CIRCUITRY

The on-chip amplifier (a digital inverter) along with an appropriate crystal may be used to provide a reference source frequency. A fundamental mode crystal, parallel resonant at the desired operating frequency, should be connected as shown in Figure A.

For V_{DD}=5 V, the crystal should be specified for a loading capacitance, C_L, which does not exceed 32 pF for frequencies to approximately 8 MHz, 20 pF for frequencies in the area of 8 to 15 MHz, and 10 pF for higher frequencies. These are guidelines that provide a reasonable compromise between IC capacitance, drive capability, swamping variations in stray and IC input/output capacitance, and realistic C_L values. The shunt load capacitance, C_L, presented across the crystal can be estimated to be:

$$C_L = \frac{C_{in}C_{out}}{C_{in}+C_{out}} + C_a + C_O + \frac{C1 \cdot C2}{C1+C2}$$

where C_{in} = 5 pF (see Figure C)
C_{out} = 6 pF (see Figure C)
C_a = 5 pF (see Figure C)
C_O = The crystal's holder capacitance (see Figure B)
C1 and C2 = External capacitors (see Figure A)

The oscillator can be "trimmed" on-frequency by making a portion or all of C1 variable. The crystal and associated components must be located as close as possible to the OSC_{in} and OSC_{out} pins to minimize distortion, stray capacitance, stray inductance, and startup stabilization time. In some cases, stray capacitance should be added to the values for C_{in} and C_{out}.

Power is dissipated in the effective series resistance of the crystal, R_e, in Figure B. The drive level specified by the crystal manufacturer is the maximum stress that a crystal can withstand without damage or excessive shift in frequency. R1 in Figure A limits the drive level. The use of R1 may not be necessary in some cases; i.e. R1 = 0 ohms.

To verify that the maximum dc supply voltage does not overdrive the crystal, monitor the output frequency as a function of voltage at OSC_{out}. (Care should be taken to minimize loading.) The frequency should increase very slightly as the dc supply voltage is increased. An overdriven crystal will decrease in frequency or become unstable with an increase in supply voltage. The operating supply voltage must be reduced or R1 must be increased in value if the overdriven condition exists. The user should note that the oscillator start-up time is proportional to the value of R1.

Through the process of supplying crystals for use with CMOS inverters, many crystal manufacturers have developed expertise in CMOS oscillator design with crystals. Discussions with such manufacturers can prove very helpful. See Table A.

TABLE A — PARTIAL LIST OF CRYSTAL MANUFACTURERS

NAME	ADDRESS	PHONE
United States Crystal Corp.	3605 McCart St., Ft. Worth, TX 76110	(817) 921-3013
Crystek Crystal	1000 Crystal Dr., Ft. Myers, FL 33906	(813) 936-2109
Statek Corp.	512 N. Main St., Orange, CA 92668	(714) 639-7810

RECOMMENDED FOR READING

Technical Note TN-24, Statek Corp.

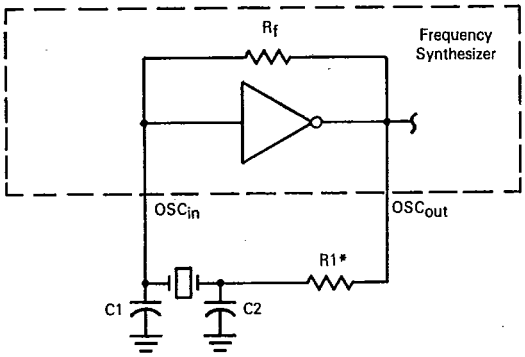
Technical Note TN-7, Statek Corp.

E. Hafner, "The Piezoelectric Crystal Unit - Definitions and Method of Measurement", *Proc. IEEE*, Vol. 57, No. 2, Feb., 1969.

D. Kemper, L. Rosine, "Quartz Crystals for Frequency Control", *Electro-Technology*, June, 1969.

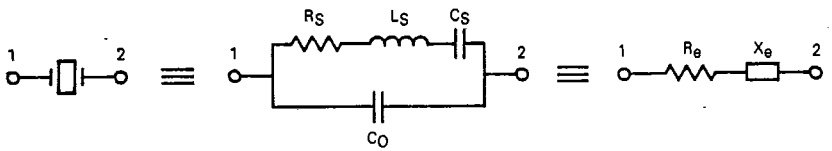
P. J. Ottowitz, "A Guide to Crystal Selection", *Electronic Design*, May, 1966.

FIGURE A — PIERCE CRYSTAL OSCILLATOR CIRCUIT



*May be deleted in certain cases. See text.

FIGURE B — EQUIVALENT CRYSTAL NETWORKS



Values are supplied by crystal manufacturer (parallel resonant crystal).

FIGURE C — PARASITIC CAPACITANCES
OF THE AMPLIFIER