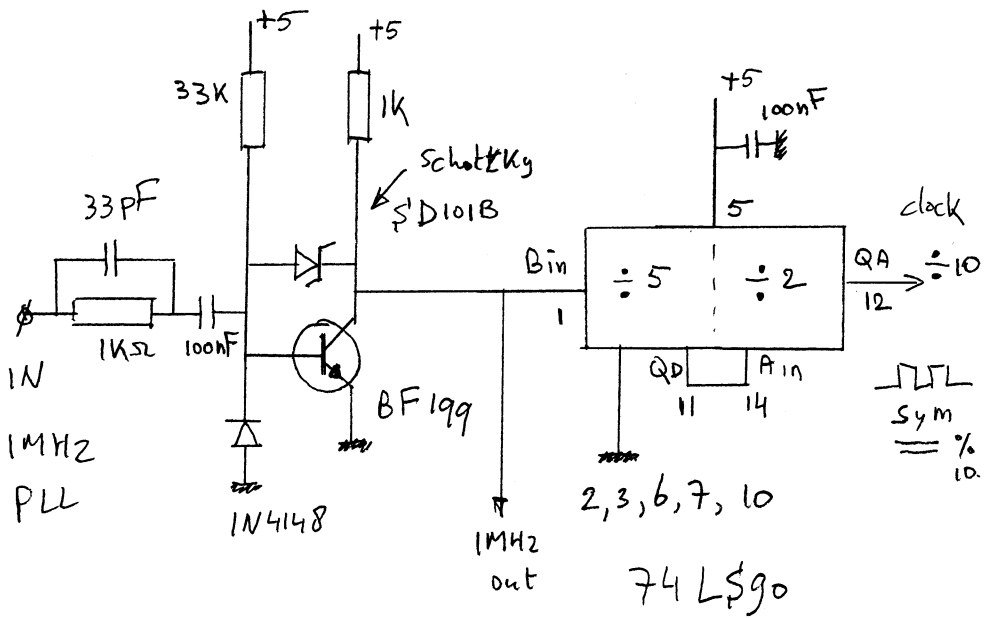




PLL clock buffer + divider

