WESTERN DIGITAL CORPORATION

MOS/LSI
TR1602A & TR1602B
ASYNCHRONOUS RECEIVER/TRANSMITTER

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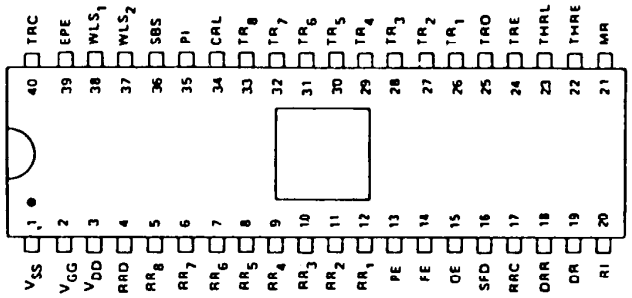
FEATURES

- SILICON GATE TECHNOLOGY – LOW THRESHOLD CIRCUITRY
  Directly TTL and DTL Compatible – External Resistors Not Required
- D. C. STABLE (STATIC) CIRCUITRY
- FULL DUPLEX OR HALF DUPLEX OPERATION
  Transmits And Receives Serial Data Simultaneously Or Alternately
- AUTOMATIC INTERNAL SYNCHRONIZATION OF DATA AND CLOCK
- AUTOMATIC START BIT GENERATION
- BUFFERED RECEIVER AND TRANSIMITTER REGISTERS
- FULLY PROGRAMMABLE – EXTERNALLY SELECTABLE
  Word Length
  Baud Rate
  Even/Odd Parity (Receiver/Verification – Transmitter/Generation)
  Party Inhibit – Verification/Generation
  One, One and One-Half, or Two Stop Bit Generation
- AUTOMATIC DATA RECEIVED/TRANSMITTED STATUS GENERATION
  Transmission Complete
  Buffer Register Transfer Complete
  Received Data Available
  Parity Error
  Framing Error
  Overrun Error
- THREE-STATE OUTPUTS
  Receiver Register Outputs
  Status Flags
- AVAILABLE IN CERAMIC OR HERMETIC PLASTIC CAVITY PACKAGES

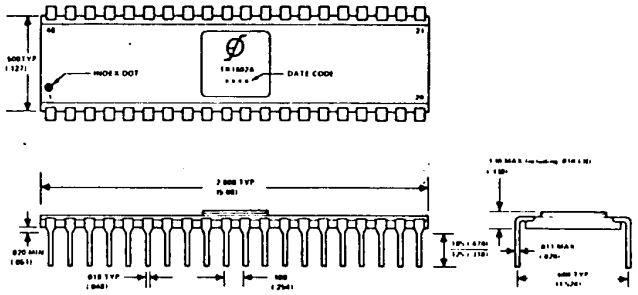
APPLICATIONS

- PERIPHERALS
- TERMINALS
- MINI COMPUTERS
- FACSIMILE TRANSMISSION
- MODEMS
- CONCENTRATORS
- ASYNCHRONOUS DATA MULTIPLEXERS
- CARD AND TAPE READERS
- PRINTERS
- DATA SETS
- CONTROLLERS
- KEYBOARD ENCODERS
- REMOTE DATA ACQUISITION SYSTEMS
- ASYNCHRONOUS DATA CASSETTES

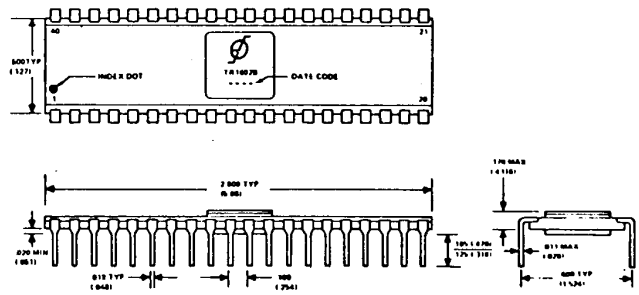
PIN CONNECTIONS



TR1602A CERAMIC PACKAGE OUTLINE



TR1602B HERMETIC PLASTIC CAVITY PACKAGE OUTLINE

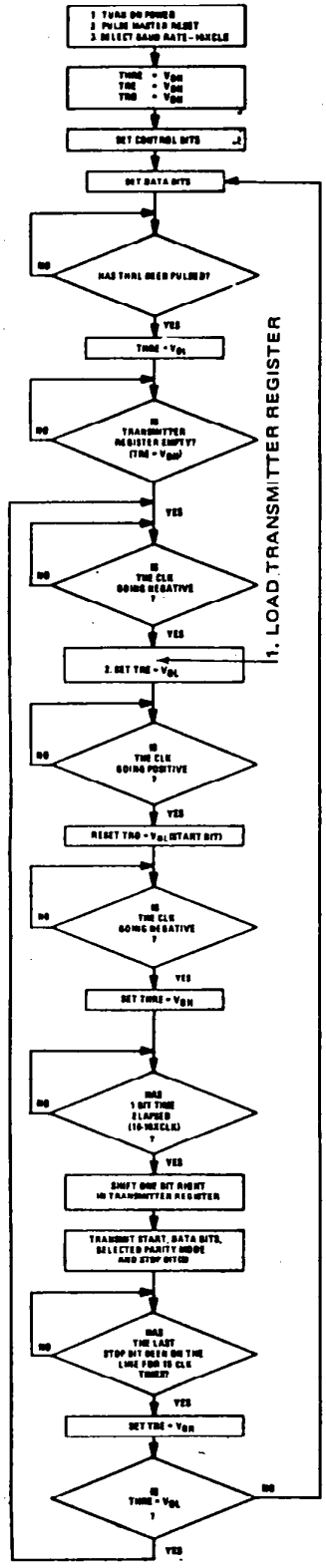


GENERAL DESCRIPTION

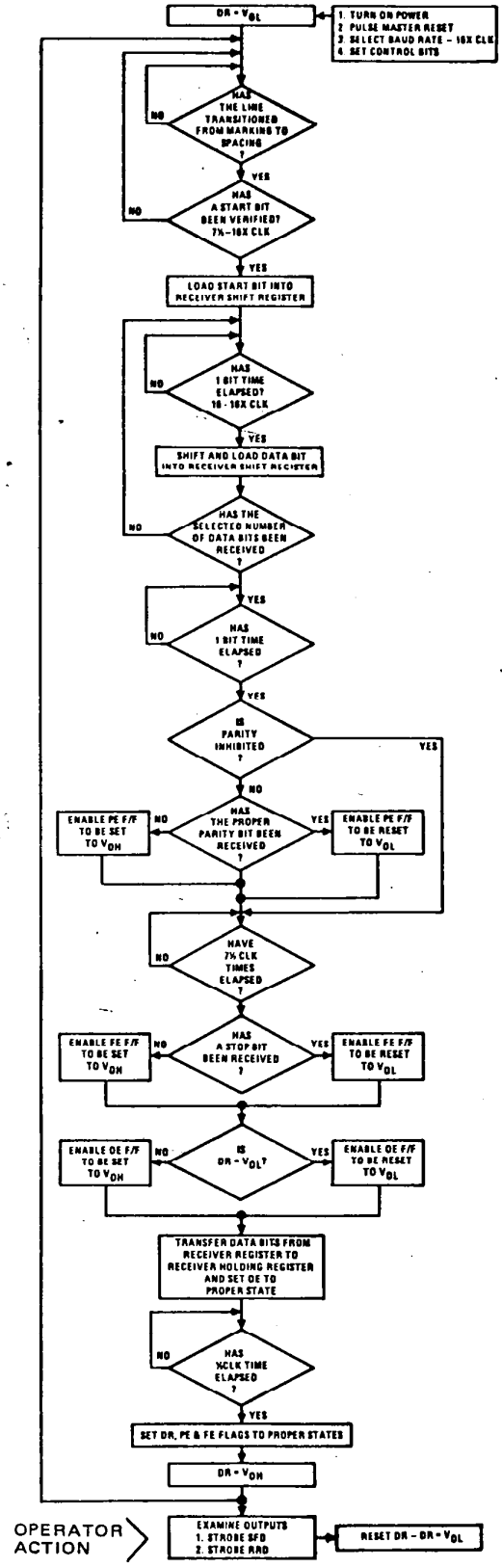
The TR1602A & the TR1602B are ASYNCHRONOUS RECEIVER/TRANSMITTER sub-systems using silicon gate process technology. The use of this low threshold process provides direct compatibility with all forms of current sinking logic. Interfacing restraints, such as external resistors, drivers and level shifting circuitry, are eliminated. All output lines have been designed to drive TTL directly.

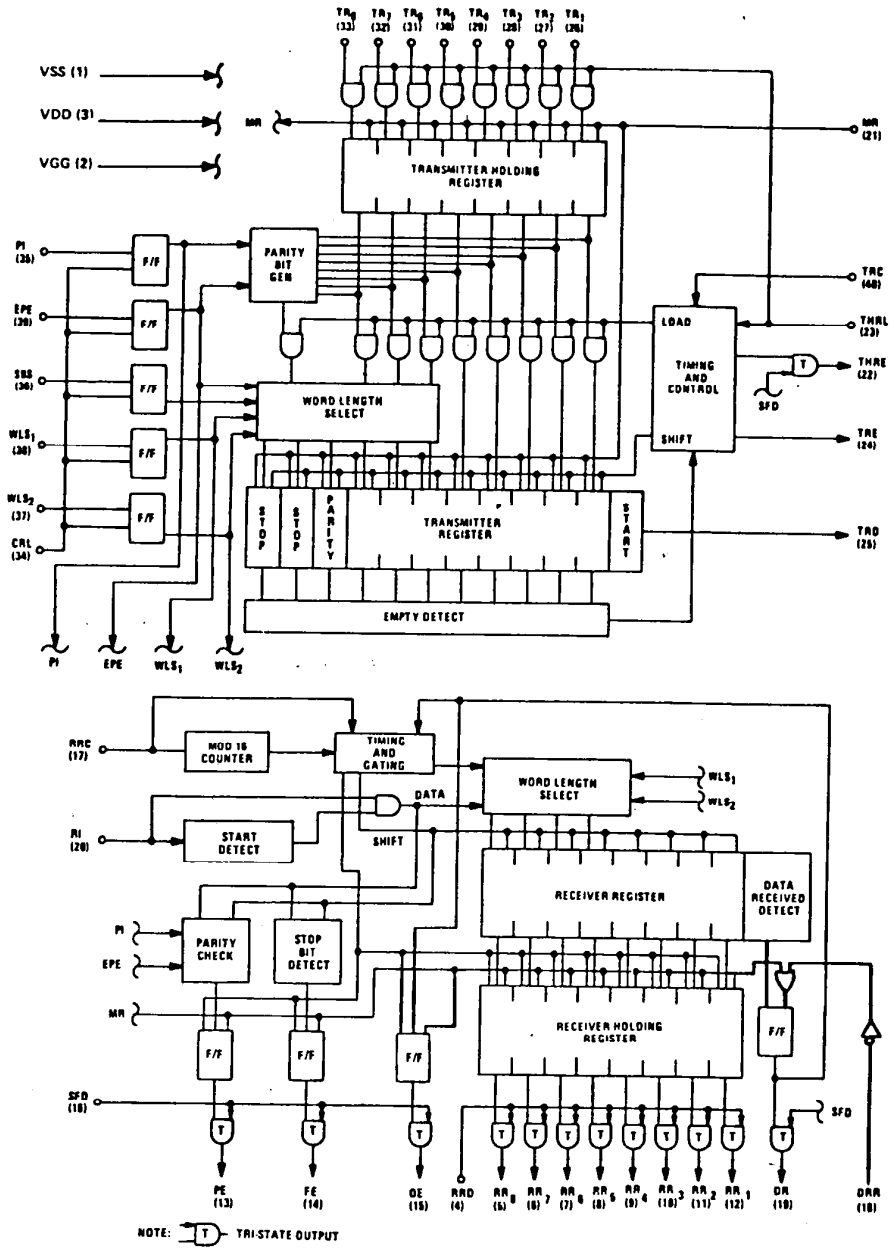
The ASYNCHRONOUS RECEIVER/TRANSMITTER is a general purpose, programmable MOS/LSI device for interfacing an asynchronous serial data channel of a peripheral or terminal with parallel data of a computer or terminal. The transmitter section converts parallel data into a serial word which contains the data along with start, parity, and stop bits. The receiver section converts a serial word with start, data, parity, and stop bits, into parallel data, and it verifies proper code transmission by checking parity and receipt of a valid stop bit. Both the receiver and the transmitter are double buffered. The array is compatible with bipolar logic. The array may be programmed as follows: The word length can be either 5, 6, 7, or 8 bits; parity generation and checking may be inhibited, the parity may be even or odd; and the number of stop bits may be either one or two, with one and one half when transmitting a 5 bit code. Note: See TR1402A Data Sheet for operation with 5 level code-2 stop bits.

TRANSMITTER FLOW CHART



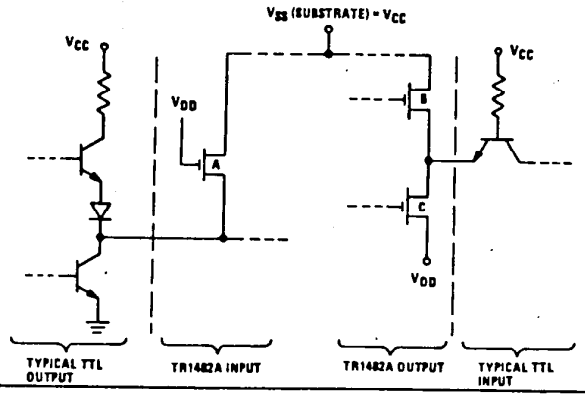
RECEIVER FLOW CHART





INPUT STRUCTURE

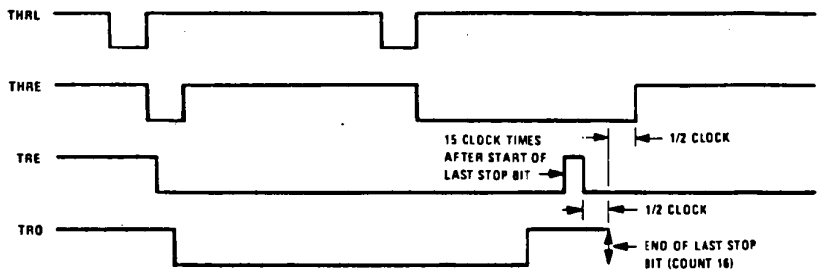
MOS DEVICE "A" ACTS AS AN INTERNAL PULL-UP RESISTOR TO $V_{SS} = V_{CC}$ WHICH BIASES OFF THE CASCODE DEVICE OF THE TTL OUTPUT IN THE HIGH-LEVEL OUTPUT STATE. IN THE LOW-LEVEL OUTPUT STATE THE TTL OUTPUT DEVICE SINKS THE CURRENT SUPPLIED BY DEVICE "A".



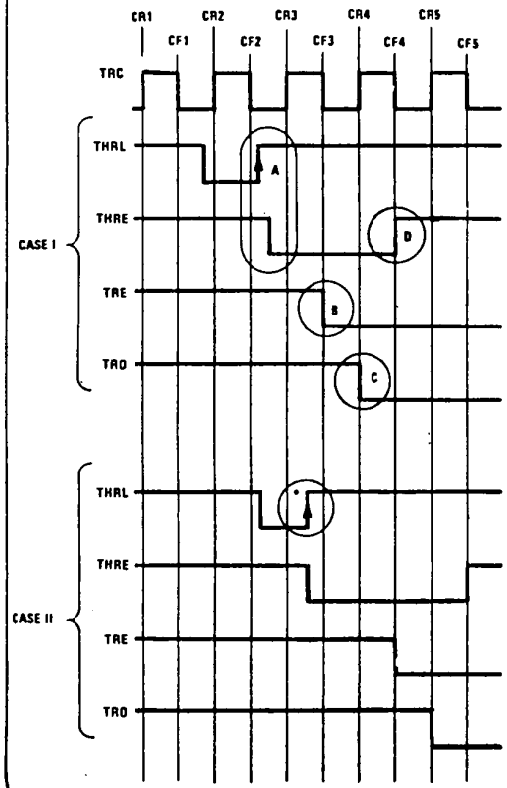
OUTPUT STRUCTURE

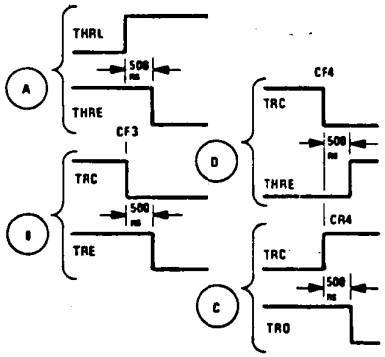
DEVICES "B" & "C" COMPRISE A PUSH-PULL OUTPUT BUFFER. IN THE LOW-LEVEL STATE, OUTPUT TRANSISTOR "C" IS "ON" AND CASCODE DEVICE "B" IS OFF. IN THE HIGH-LEVEL STATE, THE OPPOSITE IS TRUE. IN THE DISCONNECTED STATE, BOTH "B" AND "C" ARE TURNED OFF CAUSING THE OUTPUT NODE TO FLOAT.

TRANSMITTER TIMING



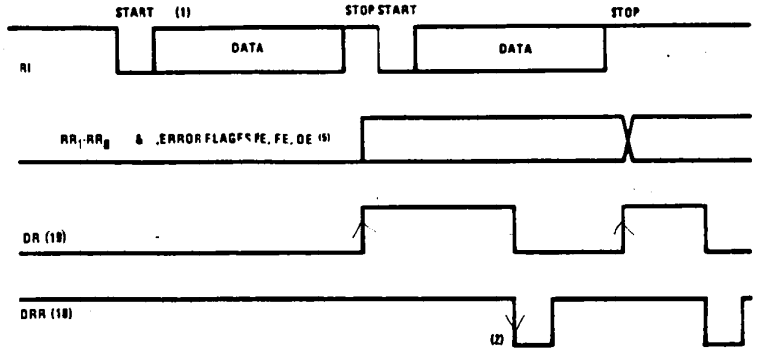
DETAIL:



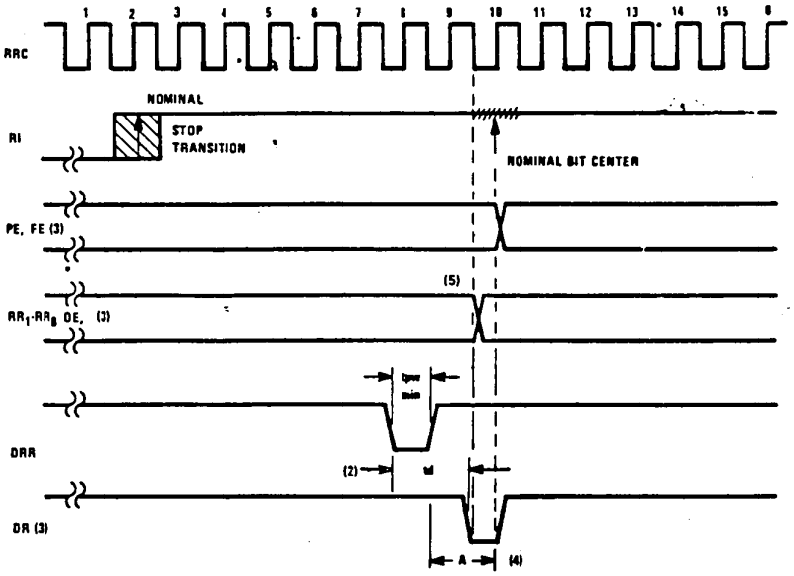


* IN CASE I, IF THE POSITIVE TRANSITION OF THRL OCCURS > 500 NS PRIOR TO ANY CF (CLOCK FALLING EDGE) THE B,C & D SIGNALS WILL BE GENERATED AS SHOWN. IN CASE II, IF THE POSITIVE TRANSITION OCCURS < 500 NS PRIOR TO CF, THE B,C & D SIGNALS MAY BE RECOGNIZED ON THE FOLLOWING CLOCK TIME. IF FOR EXAMPLE, THRL OCCURS < 500 NS BEFORE CF_3, THE B,C & D SIGNALS MAY JUMP TO CF_4, CR_5 AND CF_5, RESPECTIVELY.

RECEIVER TIMING



DETAIL:



(1) SEE APPLICATION REPORT NO. 1 FOR A DESCRIPTION OF START BIT DETECTION.
(2) THE DELAY BETWEEN DRR & DR = td = 500 NS
(3) DR, ERROR FLAGS AND DATA ARE VALID AT THE NOMINAL CENTER OF THE FIRST STOP BIT
(4) DRR SHOULD BE HIGH A MINIMUM OF "A" NS (ONE-HALF CLOCK TIME PLUS 500 NS) PRIOR TO DR RISING EDGE.
(5) DATA & OE PRECEDES DR & ERROR FLAGS BY ½ CLOCK.

PIN DEFINITIONS

PIN NUMBER	NAME	SYMBOL	FUNCTION
1	V_{SS} Power Supply	V_{SS}	+5 volts supply
2	V_{GG} Power Supply	V_{GG}	-12 volts supply
3	V_{DD} Power Supply	V_{DD}	Ground
4	Receiver Register Disconnect	RRD	A high level input voltage, V_{IH}, applied to this line disconnects the RECEIVER HOLDING REGISTER outputs from the RR_8-RR_1 data outputs (pins 5-12).
5–12	Receiver Holding Register Data	RR_8–RR_1	The parallel contents of the RECEIVER HOLDING REGISTER appear on these lines if a low-level input voltage, V_{IL}, is applied to RRD. For character formats of fewer than eight bits received characters are right-justified with RR_1 (pin 12) as the least significant bit and the truncated bits are forced to a low level output voltage, V_{OL}.
13	Parity Error	PE	A high level output voltage, V_{OH}, on this line indicates that the received parity does not compare to that programmed by the EVEN PARITY ENABLE control line (pin 39). This output is updated each time a character is transferred to the RECEIVER HOLDING REGISTER. PE lines from a number of arrays can be bussed together since an output disconnect capability is provided by Status Flag Disconnect line (pin 16).
14	Framing Error	FE	A high-level output voltage, V_{OH}, on this line indicates that the received character has no valid stop bit, ie., the bit following the parity bit (if programmed) is not a high level voltage. This output is updated each time a character is transferred to the Receiver Holding Register. FE lines from a number of arrays can be bussed together since an output disconnect capability is provided by the Status Flag Disconnect line (pin 16).
15	Overrun Error	OE	A high-level output voltage, V_{OH}, on this line indicates that the Data Received Flag (pin 19) was not reset before the next character was transferred to the Receiver Holding Register. OE lines from a number of arrays can be bussed together since an output disconnect capability is provided by the Status Flag Disconnect line (pin 16).
16	Status Flags Disconnect	SFD	A high-level input voltage, V_{IH}, applied to this pin disconnects the PE, FE, OE, DR and THRE allowing them to be buss connected.
17	Receiver Register Clock	RRC	The receiver clock frequency is sixteen (16) times the desired receiver shift rate.
18	Data Received Reset	DRR	A low-level input voltage, V_{IL}, applied to this line resets the DR line.
19	Data Received	DR	A high-level output voltage, V_{OH}, indicates that an entire character has been received and transferred to the RECEIVER HOLDING REGISTER.
20	Receiver Input	RI	Serial input data received on this line enters the RECEIVER REGISTER at a point determined by the character length, parity, and the number of stop bits. A high-level input voltage, V_{IH}, must be present when data is not being received.
21	Master Reset	MR	This line is strobed to a high-level input voltage, V_{IH}, to clear the logic. It resets the Transmitter and Receiver Registers, the Receiver Holding Register, FE, OE, PE, DRR and sets TRO, THRE, and TRE to a high-level output voltage, V_{OH}.
22	Transmitter Holding Register Empty	THRE	A high-level output Voltage, V_{OH}, on this line indicates the TRANSMITTER HOLDING REGISTER has transferred its contents to the TRANSMITTER REGISTER and may be loaded with a new character.

PIN DEFINITIONS (CONT)

PIN NUMBER	NAME	SYMBOL	FUNCTION
23	Transmitter Holding Register Load	THRL	A low-level input voltage, V_{IL}, applied to this line enters a character into the TRANSMITTER HOLDING REGISTER. A transition from a low-level input voltage, V_{IL}, to a high-level input voltage, V_{IH}, transfers the character into the TRANSMITTER REGISTER if it is not in the process of transmitting a character. If a character is being transmitted, the transfer is delayed until its transmission is completed. Upon completion, the new character is automatically transferred simultaneously with the initiation of the serial transmission of the new character.
24	Transmitter Register Empty	TRE	A high-level output voltage, V_{OH}, on this line indicates that the TRANSMITTER REGISTER has completed serial transmission of a full character including STOP bit(s). It remains at this level until the start of transmission of the next character.
25	Transmitter Register Output	TRO	The contents of the TRANSMITTER REGISTER (START bit, DATA bits, PARITY bit, and STOP bits) are serially shifted out on this line. When no data is being transmitted, this line will remain at a high-level output voltage, V_{OH}. Start of transmission is defined as the transition of the START bit from a high-level output voltage, V_{OH}, to a low-level output voltage, V_{OL}.
26–33	Transmitter Register Data Inputs	TR_1 – TR_8	The character to be transmitted is loaded into the TRANSMITTER HOLDING REGISTER on these lines with the THRL Strobe. If a character of less than 8 bits has been selected (by WLS_1 and WLS_2), the character is right justified to the least significant bit, RR1, and the excess bits are disregarded. A high-level input voltage, V_{IH}, will cause a high-level output voltage, V_{OH}, to be transmitted.
34	Control Register Load	CRL	A high-level input voltage, V_{IH}, on this line loads the CONTROL REGISTER with the control bits (WLS_1, WLS_2, EPE, PI, SBS). This line may be strobed or hard wired to a high-level input voltage, V_{IH}.
35	Parity Inhibit	PI	A high-level input voltage, V_{IH}, on this line inhibits the parity generation and verification circuits and will clamp the PE output (pin 13) to V_{OL}. If parity is inhibited the STOP bit(s) will immediately follow the last data bit on transmission.
36	Stop Bit(s) Select	SBS	This line selects the number of STOP bits to be transmitted after the PARITY bit. A high-level input voltage, V_{IH}, on this line selects two STOP bits, and a low-level input voltage, V_{IL}, selects a single STOP bit. Selection of two STOP bits when programming a five (5) bit word generates 1.5 STOP bits.
37–38	Word Length Select	WLS_2 – WLS_1	These two lines select the character length (exclusive of parity) as follows:

WLS_2	WLS_1	Word Length
V_{IL}	V_{IL}	5 bits
V_{IL}	V_{IH}	6 bits
V_{IH}	V_{IL}	7 bits
V_{IH}	V_{IH}	8 bits

39	Even Parity Enable	EPE	This line determines whether even or odd PARITY is to be generated by the transmitter and checked by the receiver. A high-level input voltage, V_{IH}, selects even PARITY and a low-level input voltage, V_{IL}, selects odd PARITY.
40	Transmitter Register Clock	TRC	The transmitter clock frequency is sixteen (16) times the desired transmitter shift rate.

MAXIMUM RATINGS

V_{GG} Supply Voltage	+0.3V	to	- 20V
V_{DD} Supply Voltage	+0.3V	to	- 20V
Clock Input Voltage*	+0.3V	to	- 20V
Logic Input Voltage*	+0.3V	to	- 20V
Logic Output Voltage*	+0.3V	to	- 20V
Storage Temperature	-55°C	to	+150°C
Operating Free-Air Temperature T_A Range	0°C	to	+ 70°C **
Lead Temperature (Soldering, 10 sec.)			300°C

*$V_{GG} = V_{DD} = 0V$

NOTE: These voltages are measured with respect to V_{SS} (Substrate)

ELECTRICAL CHARACTERISTICS

($V_{SS} = V_{CC} = 5V \pm 5\%$, $V_{DD} = 0V$, $V_{GG} = -12V \pm 5\%$, $T_A = 0°C$ to $+70°C$ unless otherwise specified)

SYM	PARAMETER	MIN	MAX	CONDITIONS
	OPERATING CURRENT			
I_{SS}	Substrate Supply Current		24 ma	$V_{SS} = 5.25V$, V_{IN} = OPEN
I_{SS}	Substrate Supply Current		60 ma	$V_{SS} = 5.25V$, $V_{IN} = +0.4V$
I_{GG}	Gate Supply Current		6 ma	
	LOGIC LEVELS			
V_{IH}	Logic High	$V_{SS} - 1.5V$		
V_{IL}	Logic Low		0.8 V	$V_{SS} = 4.75V$
	OUTPUT LOGIC LEVELS			
V_{OH}	Logic High	$V_{SS} - 1.0V$		$V_{SS} = 4.75V$, $I_{OH} = -100\mu a$
V_{OL}	Logic Low		0.4 V	$V_{SS} = 5.25V$, $I_{OL} = 1.6$ ma
I_{OS}*	Short Circuit Current		−2.2 ma	$V_{SS} = 5.25V$, $V_O = 0V$
I_{OC}	Output Leakage		$10\mu a$	$V_{OUT} = 0V$, SFD=RRD=V_{IH}
I_{IL}	Low Level Input Current		−1.6 ma	$V_{SS} = 5.25$, $V_{IN} = 0.4V$

*Only one output should be shorted at any time.

**Consult factory for extended temperature range UARTS.

SWITCHING CHARACTERISTICS – See "Switching Waveforms"

($V_{SS} = V_{CC} = 5V$, $V_{DD} = 0V$, $V_{GG} = -12V$, $T_A = 25^{\circ}$, C_{LOAD} = 20 pf plus one TTL load)

SYM	PARAMETER	MIN	MAX	CONDITIONS
f_{clock}	Clock Frequency	D.C.	320kHz*	V_{SS} = 4.75V
t_{pw}	Pulse Widths			(See figures 1 & 2)
	CRL	200 ns		
	THRL	200 ns		
	DRR	200 ns		
	MR	500 ns		
t_c	Coincidence Time	200 ns		(See figure 1 & 2)
t_{hold}	Hold Time	20 ns		(See figure 1 & 2)
t_{set}	Set Time	0		(See figure 1 & 2)
	Output Propagation Delays			
t_{pd0}	To Low State		500 ns.	(See figure 3) C_L = 20 pf, plus one TTL load
t_{pd1}	To High State		500 ns	(See figure 3) C_L = 20 pf, plus one TTL load
	Capacitance			
c_{in}	Inputs		20 pf	f = 1 MHz, V_{in} = 5V
c_o	Outputs		20 pf	f = 1 MHz, V_{in} = 5V

*f_{max} for TR1602A or B 320kHz
f_{max} for TR1602A or B-03 480kHz
f_{max} for TR1602A or B-04 640kHz
f_{max} for TR1602A or B-05 800kHz

SWITCHING WAVE FORMS

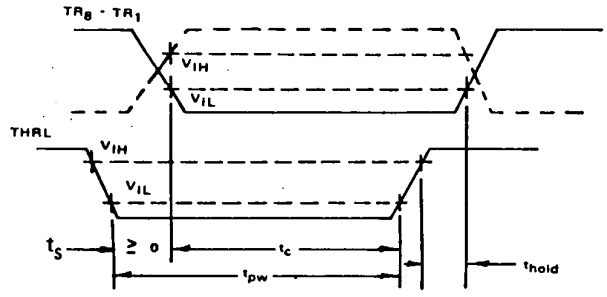


FIGURE 1. DATA INPUT LOAD CYCLE

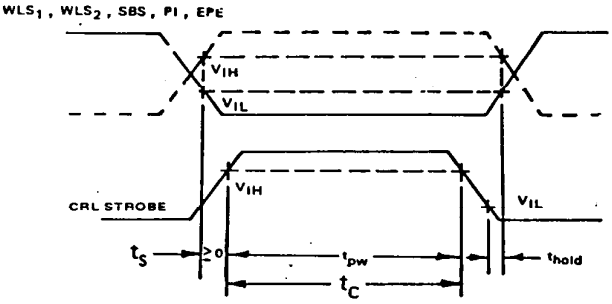
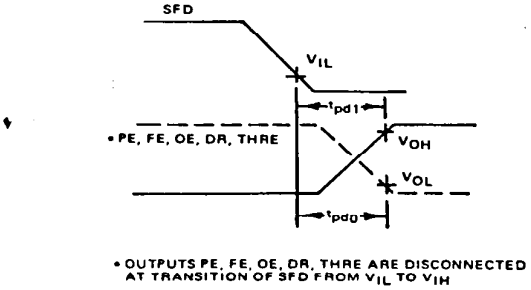
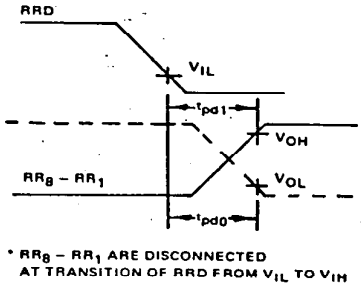


FIGURE 2. CONTROL REGISTER LOAD CYCLE



• OUTPUTS PE, FE, OE, DR, THRE ARE DISCONNECTED AT TRANSITION OF SFD FROM V_{IL} TO V_{IH}

FIGURE 3. STATUS FLAG OUTPUT DELAYS



* $RR_8 - RR_1$ ARE DISCONNECTED AT TRANSITION OF RRD FROM V_{IL} TO V_{IH}

FIGURE 4. DATA OUTPUT DELAYS