HM-6561/883

March 1997

256 x 4 CMOS RAM

Features

- **This Circuit is Processed in Accordance to MIL-STD-883 and is Fully Conformant Under the Provisions of Paragraph 1.2.1.**
- **Low Power Standby. . . . . 50μW Max**
- **Low Power Operation . . . . . .20mW/MHz Max**
- **Fast Access Time . . . . . 200ns Max**
- **Data Retention . . . . . .at 2.0V Min**
- **TTL Compatible Input/Output**
- **High Output Drive - 1 TTL Load**
- **On-Chip Address Registers**
- **Common Data In/Out**
- **Three-State Output**
- **Easy Microprocessor Interfacing**

Description

The HM-6561/883 is a 256 x 4 static CMOS RAM fabricated using self-aligned silicon gate technology. Synchronous circuit design techniques are employed to achieve high performance and low power operation.

On-chip latches are provided for address and data outputs allowing efficient interfacing with microprocessor systems. The data output buffers can be forced to a high impedance state for use in expanded memory arrays. The data inputs and outputs are multiplexed internally for common I/O bus compatibility.

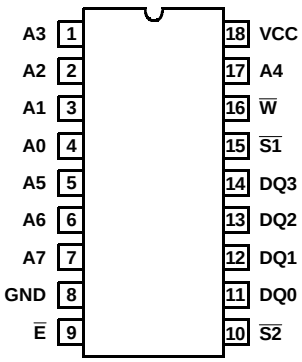
The HM-6561/883 is a fully static RAM and may be maintained in any state for an indefinite period of time. Data retention supply voltage and supply current are guaranteed over temperature.

Ordering Information

PACKAGE	TEMPERATURE RANGE	220ns	300ns	PKG. NO.
CERDIP	-55^{O}C to +125^{O}C	HM1-6561B/883	HM1-6561/883	F18.3

Pinout

HM-6561/883 (CERDIP)
TOP VIEW



PIN	DESCRIPTION
A	Address Input
$\overline{E}$	Chip Enable
$\overline{W}$	Write Enable
$\overline{S}$	Chip Select
DQ	Data In/Out

CAUTION: These devices are sensitive to electrostatic discharge; follow proper IC Handling Procedures.
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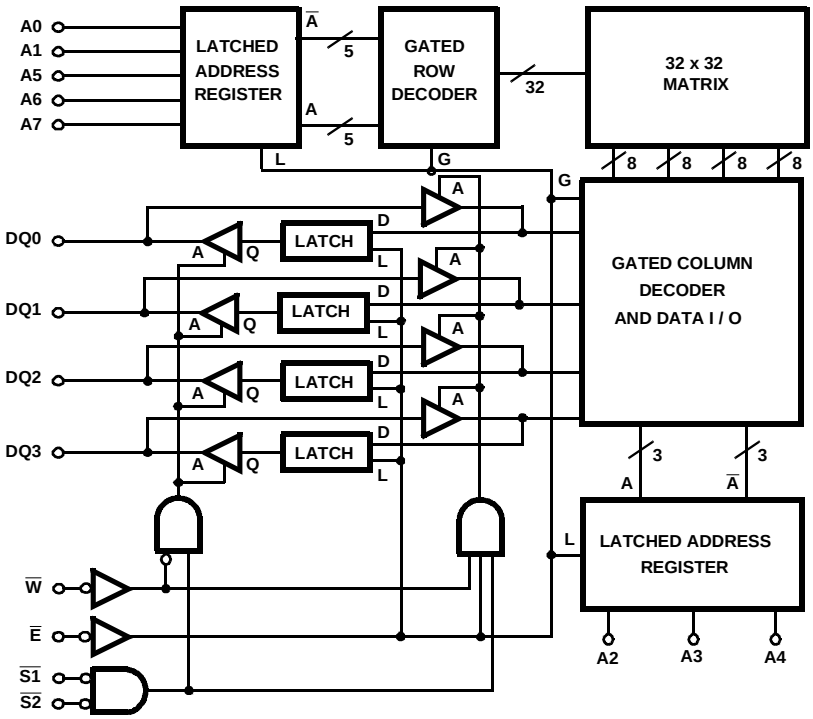
Functional Diagram



NOTES:

1. All lines positive logic-active high.
2. Three-state Buffers: A high $\rightarrow$ output active.
3. Data Latches: L high $\rightarrow$ Q = D and Q latches on falling edge of L.
4. Address Latches and Gated Decoders: Latch on falling edge of $\overline{E}$ and gate on falling edge of $\overline{E}$.

Absolute Maximum Ratings

Supply Voltage . . . . . +7.0V
Input or Output Voltage . . . . . GND -0.3V to VCC +0.3V
ESD Classification . . . . . Class 1

Thermal Information

Thermal Resistance	θ_{JA}	θ_{JC}
CERDIP Package	$74^oC/W$	$18^oC/W$

Maximum Storage Temperature Range . . . . . -65^oC to $+150^oC$
Maximum Junction Temperature. . . . . $+175^oC$
Maximum Lead Temperature (Soldering 10s). . . . . $+300^oC$

Die Characteristics

Gate Count . . . . . 1944 Gates

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Operating Voltage Range . . . . . +4.5V to +5.5V
Operating Temperature Range. . . . . -55^oC to $+125^oC$
Input Low Voltage. . . . . 0V to +0.8V
Input High Voltage. . . . . VCC - 2.0V to VCC
Input Rise and Fall Time . . . . . 40ns Max

TABLE 1. HM-6561/883 DC ELECTRICAL PERFORMANCE SPECIFICATIONS

Device Guaranteed and 100% Tested

PARAMETER	SYMBOL	(NOTE 1) CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Output Low Voltage	VOL	VCC = 4.5V, IOL = 1.6mA	1, 2, 3	$-55^oC \le T_A \le +125^oC$	-	0.4	V
Output High Voltage	VOH	VCC = 4.5V, IOH = -0.4mA	1, 2, 3	$-55^oC \le T_A \le +125^oC$	2.4	-	V
Input Leakage Current	II	VCC = 5.5V, VI = GND or VCC	1, 2, 3	$-55^oC \le T_A \le +125^oC$	-1.0	+1.0	µA
Input/Output Leakage Current	IIOZ	VCC = 5.5V, VIO = GND or VCC	1, 2, 3	$-55^oC \le T_A \le +125^oC$	-1.0	+1.0	µA
Data Retention Supply Current	ICCDR	VCC = 2.0V, $\overline{E}$ = VCC, IO = 0mA,	1, 2, 3	$-55^oC \le T_A \le +125^oC$	-	10	µA
Operating Supply Current	ICCOP	VCC = 5.5V, (Note 2), $\overline{E}$ = 1MHz, $\overline{W}$ = GND, VI = VCC or GND	1, 2, 3	$-55^oC \le T_A \le +125^oC$	-	4	mA
Standby Supply Current	ICCSB	VCC = 5.5V, IO = 0mA, VI = VCC or GND	1, 2, 3	$-55^oC \le T_A \le +125^oC$	-	10	µA

NOTES:

1. All voltages referenced to device GND.
2. Typical derating 1.5mA/MHz increase in ICCOP.

TABLE 2. HM-6561/883 A.C. ELECTRICAL PERFORMANCE SPECIFICATIONS

Device Guaranteed and 100% Tested

PARAMETER	SYMBOL	(NOTES 1, 2) CONDITIONS	GROUP A SUB-GROUPS	TEMPERATURE	LIMITS				UNITS
					HM-6561B/883		HM-6561/883		
					MIN	MAX	MIN	MAX	
Chip Enable Access Time	(1) TELQV	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	-	220	-	300	ns
Address Access Time	(2) TAVQV	VCC = 4.5 and 5.5V, (Note 3)	9, 10, 11	$-55^oC \le T_A \le +125^oC$	-	220	-	300	ns
Chip Select Output Enable Time	(3) TSLQX	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	5	-	5	-	ns
Chip Select Output Disable Time	(4) TSHQZ	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	-	120	-	150	ns
Chip Enable Pulse Negative Width	(5) TELEH	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	220	-	300	-	ns
Chip Enable Pulse Positive Width	(6) TEHEL	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	100	-	100	-	ns
Address Setup Time	(7) TAVEL	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	0	-	0	-	ns
Address Hold Time	(8) TELAX	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	40	-	50	-	ns
Data Setup Time	(9) TDVWH	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	100	-	150	-	ns
Data Hold Time	(10) TWHDX	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	0	-	0	-	ns
Write Data Delay Time	(11) TWLDV	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	20	-	30	-	
Chip Select Write Pulse Setup Time	(12) TWLSH	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	120	-	180	-	ns
Chip Enable Write Pulse Setup Time	(13) TWLEH	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	120	-	180	-	ns
Chip Select Write Pulse Hold Time	(14) TSLWH	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	120	-	180	-	ns
Chip Enable Write Pulse Hold Time	(15) TELWH	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	120	-	180	-	ns
Write Enable Pulse Width	(16) TWLWH	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	120	-	180	-	ns
Read or Write Cycle Time	(17) TELEL	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	320	-	400	-	ns

NOTES:

1. All voltages referenced to device GND.
2. Input pulse levels: 0.8V to VCC-2.0V; Input rise and fall times: 5ns (max); Input and output timing reference level: 1.5V; Output load: IOL = 1.6mA, IOH = -0.4mA, CL = 50pF (min) - for CL greater than 50pF, access time is derated by 0.15ns per pF.
3. TAVQV = TELQV + TAVEL.

TABLE 3. HM-6561/883 ELECTRICAL PERFORMANCE SPECIFICATIONS

SYMBOL	PARAMETER	CONDITIONS	NOTE	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
CI	Input Capacitance	VCC = Open, f = 1MHz, All Measurements Referenced to Device Ground	1	$T_A = +25^oC$	-	8	pF
CO	Output Capacitance	VCC = Open, f = 1MHz, All Measurements Referenced to Device Ground	1	$T_A = +25^oC$	-	10	pF

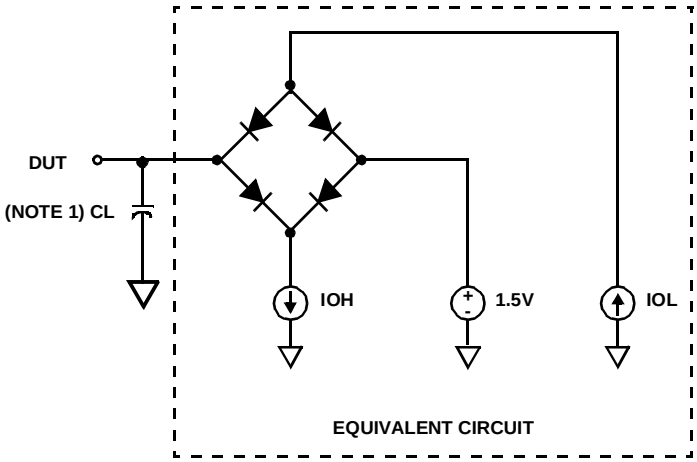
NOTE:

1. The parameters listed in Table 3 are controlled via design or process parameters are characterized upon initial design and after major process and/or design changes.

TABLE 4. APPLICABLE SUBGROUPS

CONFORMANCE GROUPS	METHOD	SUBGROUPS
Initial Test	100%/5004	-
Interim Test	100%/5004	1, 7, 9
PDA	100%/5004	1
Final Test	100%/5004	2, 3, 8A, 8B, 10, 11
Group A	Samples/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11
Groups C & D	Samples/5005	1, 7, 9

Test Load Circuit



NOTE:

1. Test head capacitance includes stray and jig capacitance.

Timing Waveforms

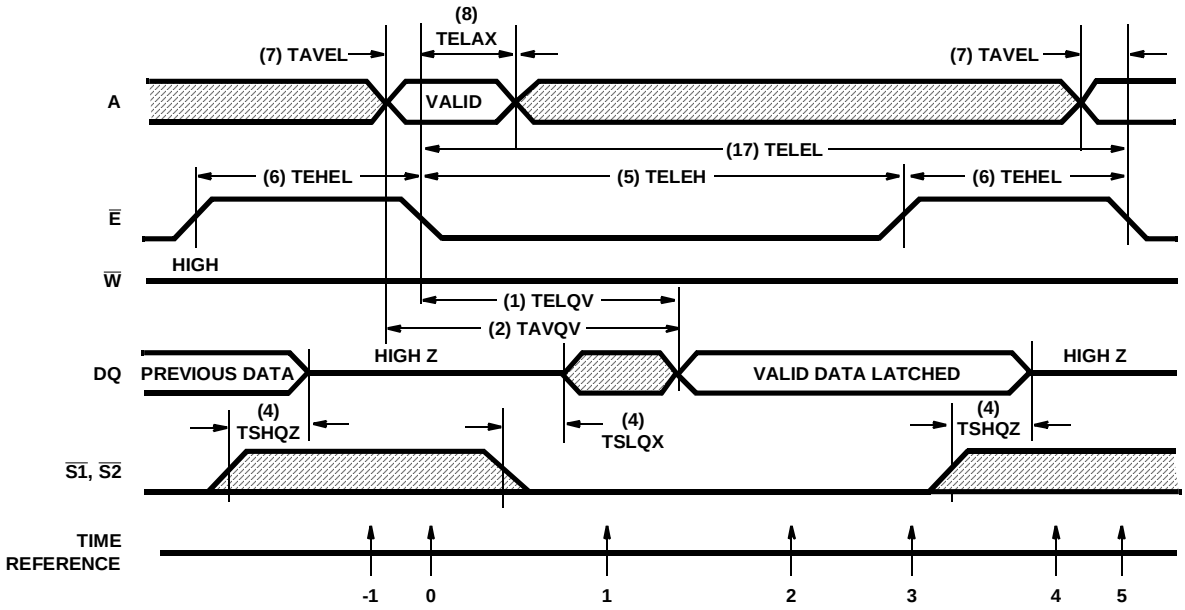


FIGURE 1. READ CYCLE

TRUTH TABLE

TIME REFERENCE	INPUTS				OUTPUT	FUNCTION
	$\overline{E}$	$\overline{S1}$	$\overline{W}$	A	DQ	
-1	H	H	X	X	Z	Memory Disabled
0	↘	X	H	V	Z	Cycle Begins, Addresses are Latched
1	L	L	H	X	X	Output Enabled
2	L	L	H	X	V	Output Valid
3	↗	L	H	X	V	Output Latched
4	H	H	X	X	Z	Device Disabled, Prepare for Next Cycle (Same as -1)
5	↘	X	H	V	Z	Cycle Ends, Next Cycle Begins (Same as 0)

NOTE: 1. Device selected only if both $\overline{S1}$ and $\overline{S2}$ are low, and deselected if either $\overline{S1}$ or $\overline{S2}$ are high.

The HM-6561/883 Read Cycle is initiated on the falling edge of $\overline{E}$. This signal latches the input address word into on-chip registers. Minimum address setup and hold times must be met. After the required hold time, the address lines may change state without affecting device operation. In order to read the output data $\overline{E}$, $\overline{S1}$ and $\overline{S2}$ must be low and $\overline{W}$ must be high. The output data will be valid at access time (TELQV).

The HM-6561/883 has output data latches that are controlled by $\overline{E}$. On the rising edge of $\overline{E}$ the present data is latched and remains latched until $\overline{E}$ falls. Either or both $\overline{S1}$ or $\overline{S2}$ may be used to force the output buffers into a high impedance state.

Timing Waveforms (Continued)

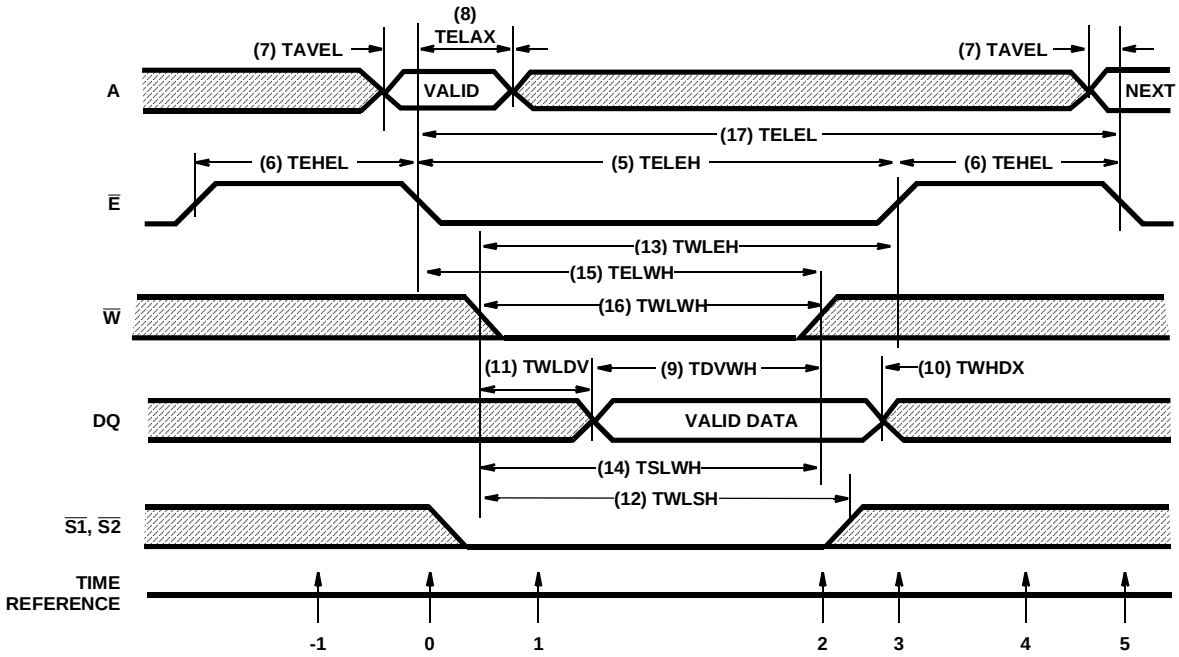


FIGURE 2. WRITE CYCLE

TRUTH TABLE

TIME REFERENCE	INPUTS					FUNCTION
	$\overline{E}$	$\overline{S1}$	$\overline{W}$	A	DQ	
-1	H	H	X	X	X	Memory Disabled
0	↓	X	X	V	X	Cycle Begins, Addresses are Latched
1	L	L	L	X	X	Write Period Begins
2	L	L	↑	X	V	Data In is Written
3	↑	X	H	X	X	Write is Completed
4	H	H	X	X	X	Prepare for Next Cycle (Same as -1)
5	↓	X	X	V	X	Cycle Ends, Next Cycle Begins (Same as 0)

NOTE: 1. Device selected only if both $\overline{S1}$ and $\overline{S2}$ are low, and deselected if either $\overline{S1}$ or $\overline{S2}$ are high.

The write cycle begins with the $\overline{E}$ falling edge latching the address. The write portion of the cycle is defined by $\overline{E}$, $\overline{S1}$, $\overline{S2}$ and $\overline{W}$ all being low simultaneously. The write portion of the cycle is terminated by the first rising edge of any control line, $\overline{E}$, $\overline{S1}$, $\overline{S2}$ or $\overline{W}$. The data setup and data hold times (TDVWH and TWHDX) must be referenced to the terminating signal. For example, if $\overline{S2}$ rises first, data setup and hold times become TDVS2H and TS2HDX; and are numerically equal to TDVWH and TWHDX.

Data input/output multiplexing is controlled by $\overline{W}$. Care must be taken to avoid data bus conflicts, where the RAM outputs become enabled when another device is driving the data inputs. The following two examples illustrate the timing required to avoid bus conflicts.

Case 1: Both $\overline{S1}$ and $\overline{S2}$ Fall Before $\overline{W}$ Falls.

If both selects fall before $\overline{W}$ falls, the RAM outputs will become enabled. $\overline{W}$ is used to disable the outputs, so a disable time (TWLQZ = TWLDV) must pass before any other device can begin to drive the data inputs. This method of operation requires a wider write pulse, because TWLDV + TDVWH is greater than TWLWH. In this case TWLSL + TSHWH are meaningless and can be ignored.

Case 2: $\overline{W}$ Falls Before Both $\overline{S1}$ and $\overline{S2}$ Fall.

If one or both selects are high until $\overline{W}$ falls, the outputs are guaranteed not to enable at the beginning of the cycle. This eliminates the concern for data bus conflicts and simplifies data input timing. Data input may be applied as early as convenient, and TWLDV is ignored. Since $\overline{W}$ is not used to disable the outputs it can be shorter than in Case 1; TWLWH is the minimum write pulse. At the end of the write period, if $\overline{W}$ rises before either select the outputs will enable reading data just written. They will not disable until either select goes high (TSHQZ).

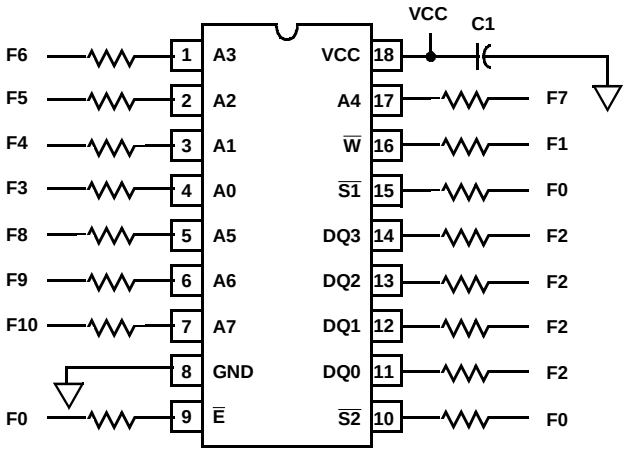
	IF	OBSERVE	IGNORE
CASE 1	Both $\overline{S1}$ and $\overline{S2}$ = Low Before $\overline{W}$ = Low	TWLQZ TWLDV TDVWH	TWLWH
CASE 2	$\overline{W}$ = Low Before Both $\overline{S1}$ and $\overline{S2}$ = Low	TWLWH TDVWH	TWLQZ TWLDV

If a series of consecutive write cycles are to be performed, $\overline{W}$ may remain low until all desired locations are written. This is an extension of Case 2.

Read-Modify-Write cycles and Read-Write-Read cycles can

Burn-In Circuit

HM-6561/883
CERDIP



NOTES:

All resistors 47kΩ ±5%.

F0 = 100kHz ±10%.

F1 = F0 ÷ 2, F2 = F1 ÷ 2, F3 = F2 ÷ 2 . . . F12 = F11 ÷ 2.

VCC = 5.5V ±0.5V.

VIH = 4.5V ±10%.

VIL = -0.2V to +0.4V.

C1 = 0.01µF Min.

Die Characteristics

DIE DIMENSIONS:
132 x 160 x 19 ±1mils

METALLIZATION:
Type: Si - Al
Thickness: 11kÅ ±2kÅ

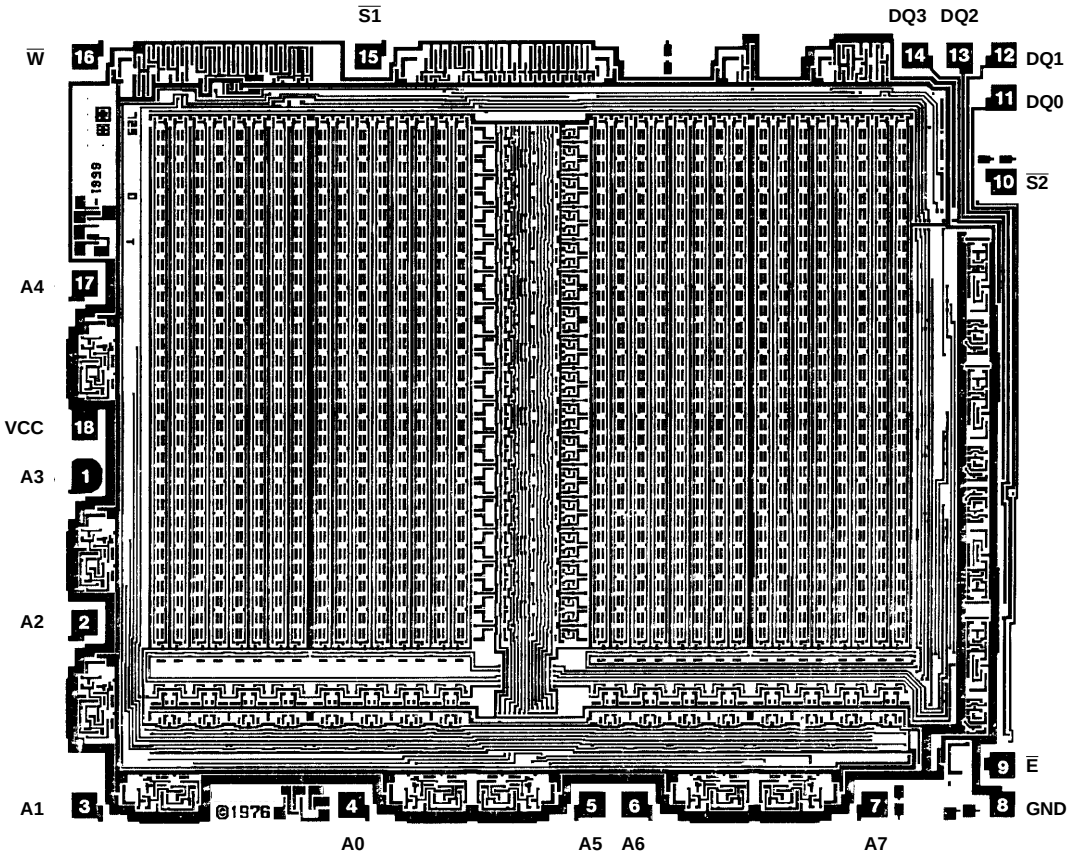
GLASSIVATION:
Type: SiO_2
Thickness: 8kÅ ±1kÅ

WORST CASE CURRENT DENSITY:
1.337 x 10^5 A/cm^2

LEAD TEMPERATURE (10s soldering):
≤ 300^oC

Metallization Mask Layout

HM-6561/883



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