



# MOS ROMs

MM4240/MM5240

## MM4240/MM5240 2560-bit static character generator general description

The MM4240/MM5240 2560-bit static character generator is a P-channel enhancement mode monolithic MOS integrated circuit utilizing a low threshold voltage technology. Six character address and three row address input lines provide access to 64-8 x 5 characters. Customer-generated single or multiple package character fonts are easily programmed by completing a pattern selection form. A standard 7 x 5 raster scan font is available by ordering the MM4240AA/MM5240AA.

The MM4240/MM5240 may be used as a 512 x 5-bit read only memory for applications other than character generation.

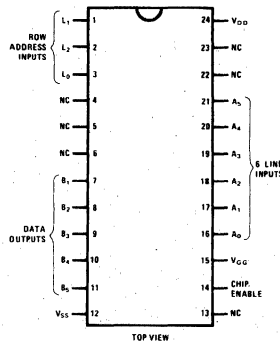
## features

- Bipolar compatibility
- High speed operation—500 ns max
- ±12 volt power supplies
- Static operation—no clocks required
- Multiple ROM logic application—chip enable output control
- Standard fonts available—off-the-shelf delivery

## applications

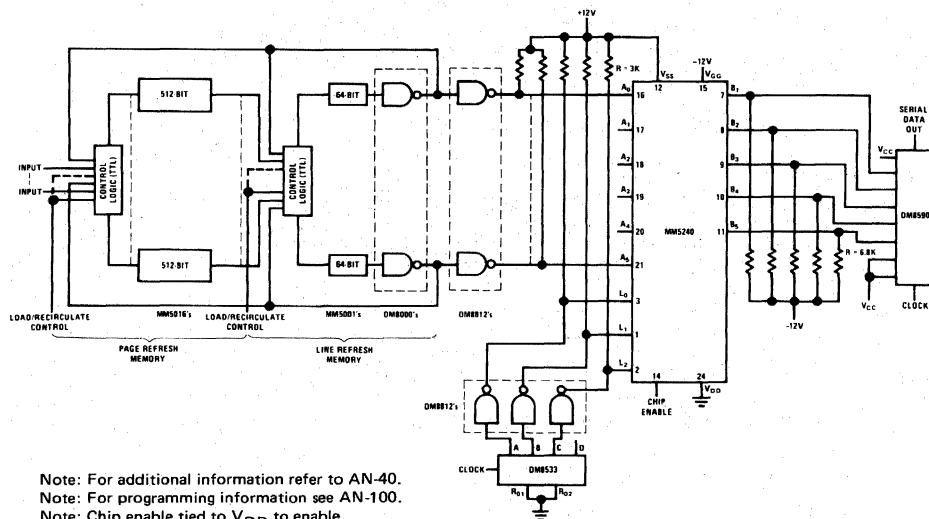
- Character generation
- Random logic synthesis
- Micro-programming
- Table look-up

## connection diagram



Order Number MM4240J or MM5240J  
See Package 11  
Order Number MM5240N  
See Package 18

## typical application



Note: For additional information refer to AN-40.  
Note: For programming information see AN-100.  
Note: Chip enable tied to  $V_{DD}$  to enable.

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**absolute maximum ratings**

$V_{GG}$ Supply Voltage	$V_{SS} - 30V$
$V_{DD}$ Supply Voltage	$V_{SS} - 15V$
Input Voltage	$(V_{SS} - 20)V < V_{IN} < (V_{SS} + 0.3)V$
Storage Temperature	$-65^{\circ}C$ to $+150^{\circ}C$
Operating Temperature	MM4240 $-55^{\circ}C$ to $+125^{\circ}C$
	MM5240 $0^{\circ}C$ to $+70^{\circ}C$
Lead Temperature (Soldering, 10 sec)	$300^{\circ}C$

**electrical characteristics** (Note 1)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Output Voltage Levels					
MOS to MOS					
Logical "1"	$1M\Omega$ to GND			$V_{SS} - 9.0$	V
Logical "0"		$V_{SS} - 1.0$			V
MOS to TTL					
Logical "1"	$6.8\ k\Omega$ to $V_{GG}$ Plus One			$+0.4$	V
Logical "0"	Standard Series 54/74 Gate	$+2.5$			V
Output Current Capability					
Logical "0"	$V_{OUT} = V_{SS} - 6.0V$	$2.5$			mA
Input Voltage Levels					
Logical "1"				$V_{SS} - 8.0$	V
Logical "0"		$V_{SS} - 2.0$			V
Power Supply Current	$T_A = 25^{\circ}C$				
$I_{DD}$	MOS Load		$25$	$40$	mA
$I_{GG}$ (Note 2)				$1$	$\mu A$
Input Leakage	$V_{IN} = V_{SS} - 12V$			$1$	$\mu A$
Input Capacitance (Note 5)	$f = 1.0\ MHz, V_{IN} = 0V$		$5$	$8$	pF
$V_{GG}$ Capacitance (Note 5)	$f = 1.0\ MHz, V_{IN} = 0V$		$25$	$40$	pF
Address Time (Note 3)	See Timing Diagram				
$T_{ACCESS}$	$T_A = 25^{\circ}C$	$150$	$425$	$500$	ns
Output AND Connection (Note 4)	MOS Load			$4$	
	TTL Load			$10$	

**Note 1:** These specifications apply for  $V_{SS} = +12V \pm 5\%$ ,  $V_{GG} = -12V \pm 5\%$ , and  $T_A = -55^{\circ}C$  to  $+125^{\circ}C$  (MM4240);  $T_A = 0^{\circ}C$  to  $+70^{\circ}C$  (MM5240) unless otherwise specified.

**Note 2:** The  $V_{GG}$  supply may be clocked to reduce device power without affecting access time.

**Note 3:** Address time is measured from the change of data on any input or Chip Enable line to the output of a TTL gate. (See Timing Diagram). See curves for guaranteed limit over temperature.

**Note 4:** The address time in the TTL load configuration follows the equation:

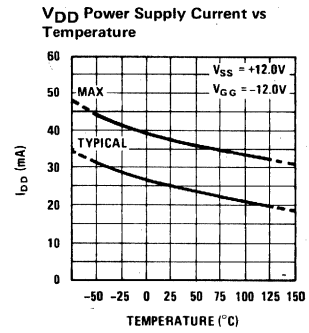
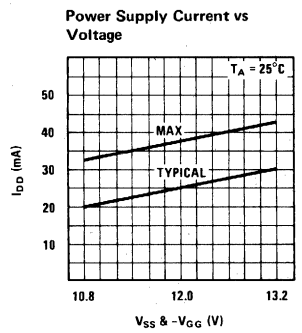
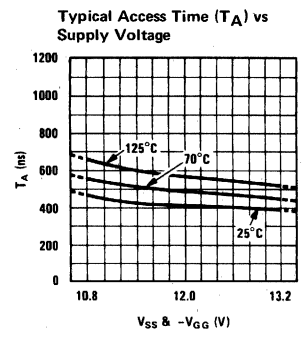
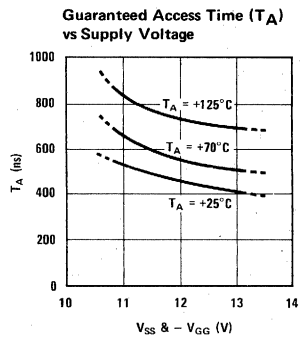
$$T_{ACCESS} = \text{The specified limit} + (N - 1) (50) \text{ ns}$$

Where N = Number of AND connections.

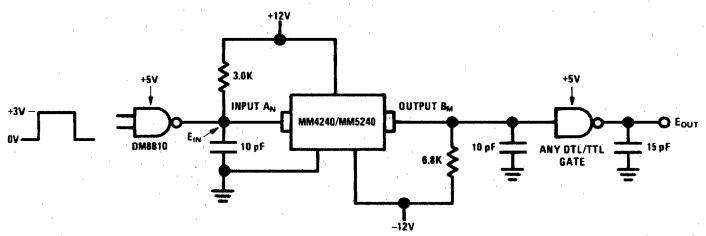
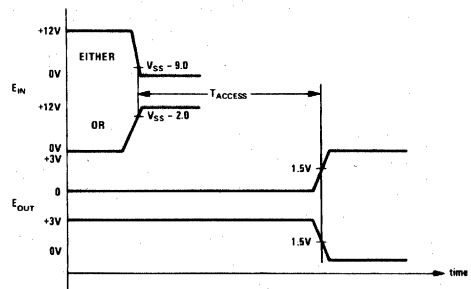
The number of AND ties in the MOS load configuration can be increased at the expense of MOS "0" level.

**Note 5:** Guaranteed by design.

performance characteristics



timing diagram/address time



# MM4240AA/MM5240AA character font

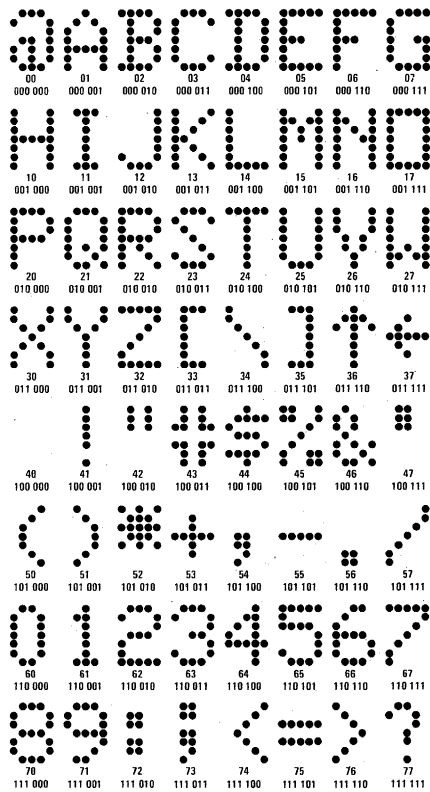
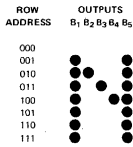


FIGURE 4

Note: Negative logic assumed.



# MOS ROMs

MM4240ABU/MM5240ABU

## MM4240ABU/MM5240ABU hollerith character generator

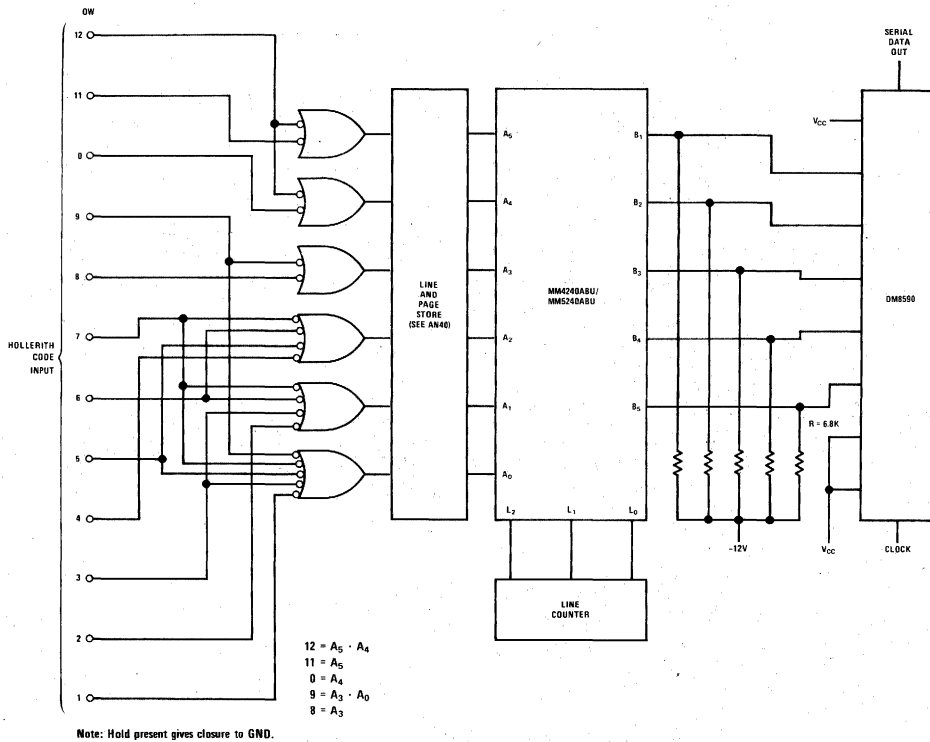
### general description

The MM4240ABU/MM5240ABU is a 64 x 8 x 5 read-only memory programmed to display a 64-character subset of the Hollerith 12-line code, normally used in punching 80 column cards. Compression from 12 lines to the six needed to make

up a 64-character set may be accomplished as shown in the typical application.

For electrical, environmental and mechanical details, refer to the MM4240/MM5240 data sheet.

### typical application



Order Number MM4240ABU/J or MM5240ABU/J  
 See Package 11  
 Order Number MM5240ABU/N  
 See Package 18

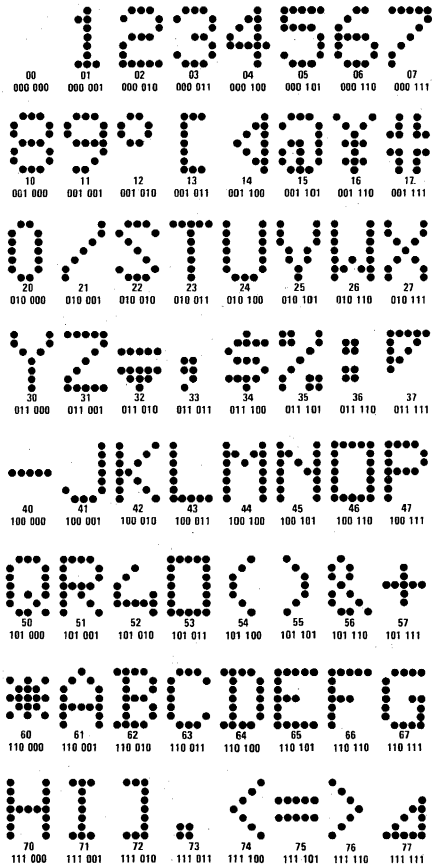
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code table

character font

HOLLERITH INPUT CODE (NON-COMPRESSED)	OCTAL SEQUENCE	GRAPHIC DISPLAY	
	00	(space)	
	1	1	
	2	2	
	3	3	
	4	4	
	5	5	
	6	6	
	7	7	
	8	8	
9	10	8	
	11	9	
8	2	12	
8	3	13	
8	4	14	
8	5	15	
8	6	16	
8	7	17	
	20		
0	21	0	
0	1	/	
0	2	S	
0	3	T	
0	4	U	
0	5	V	
0	6	W	
0	7	X	
0	8	Y	
0	9	31	
0	8	2	32
0	8	3	33
0	8	4	34
0	8	5	35
0	8	6	36
0	8	7	37
11		40	
11	1	41	
11	2	42	
11	3	43	
11	4	44	
11	5	45	
11	6	46	
11	7	47	
11	8	50	
11	9	51	
11	8	2	52
11	8	3	53
11	8	4	54
11	8	5	55
11	8	6	56
11	8	7	57
12		60	
12	1	61	
12	2	62	
12	3	63	
12	4	64	
12	5	65	
12	6	66	
12	7	67	
12	8	70	
12	9	71	
12	8	2	72
12	8	3	73
12	8	4	74
12	8	5	75
12	8	6	76
12	8	7	77
		(period)	

MM4240ABU/MM5240ABU





# MOS ROMs

MM4240ABZ/MM5240ABZ

## MM4240ABZ/MM5240ABZ EBCDIC-8 character generator

### general description

The MM4240ABZ/MM5240ABZ is a 64 x 8 x 5 read only memory that has been programmed to display the 64 character graphic subset of EBCDIC-8, an Extended Binary Coded Decimal Interchange Code with character assignments and locations conforming to the American Standard x 3.26-1970 (see MM5230QX data sheet for full EBCDIC-8 table).

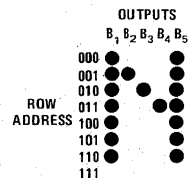
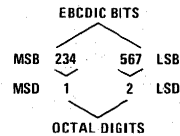
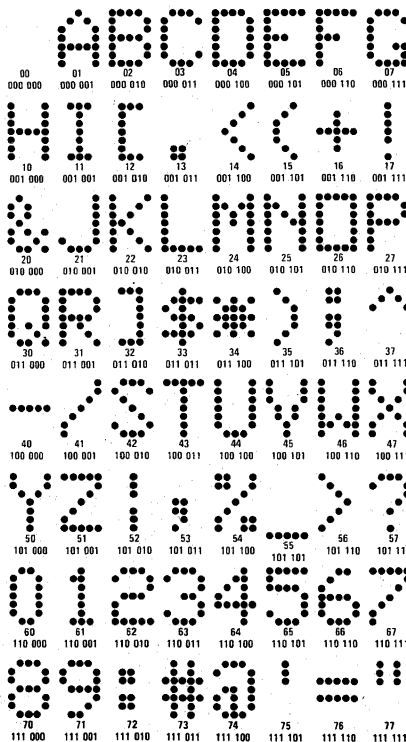
Compression of the eight bits of EBCDIC-8 to the

six needed for a 64-character subset is accomplished by simply ignoring the two most significant EBCDIC bits, bit 0 and bit 1.

The octal character address digits are then formed as shown below.

For electrical, environmental and mechanical details, refer to the MM4240/MM5240 data sheet.

### character font



Order Number MM4240ABZ/J or MM5240ABZ/J  
See Package 11

Order Number MM5240ABZ/N  
See Package 18

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# MOS ROMs

## MM4240ACA/MM5240ACA EBCDIC character generator

### general description

The MM4240ACA/MM5240ACA is a 64 x 8 x 5 read only memory that has been programmed to display the 64 character graphic subset of EBCDIC, an Extended Binary Coded Decimal Interchange code typically used in IBM systems.

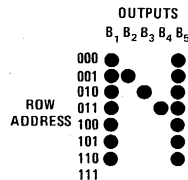
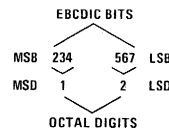
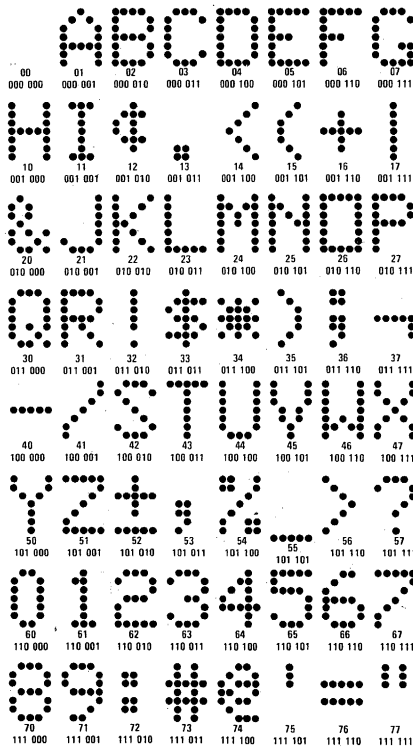
Compression of the eight bits of EBCDIC to the six needed for a 64-character subset is accom-

plished by simply ignoring the two most significant EBCDIC bits, bit zero and bit one.

The octal character address digits are then formed as shown below.

For electrical, environmental and mechanical details, refer to the MM4240/MM5240 data sheet.

### character font



Order Number MM4240ACA/J or MM5240ACA/J  
See Package 11

Order Number MM5240ACA/N  
See Package 18